



Design Verification to Application Validation of a Multiprocessor SoC

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DSP Systems

Texas Instruments

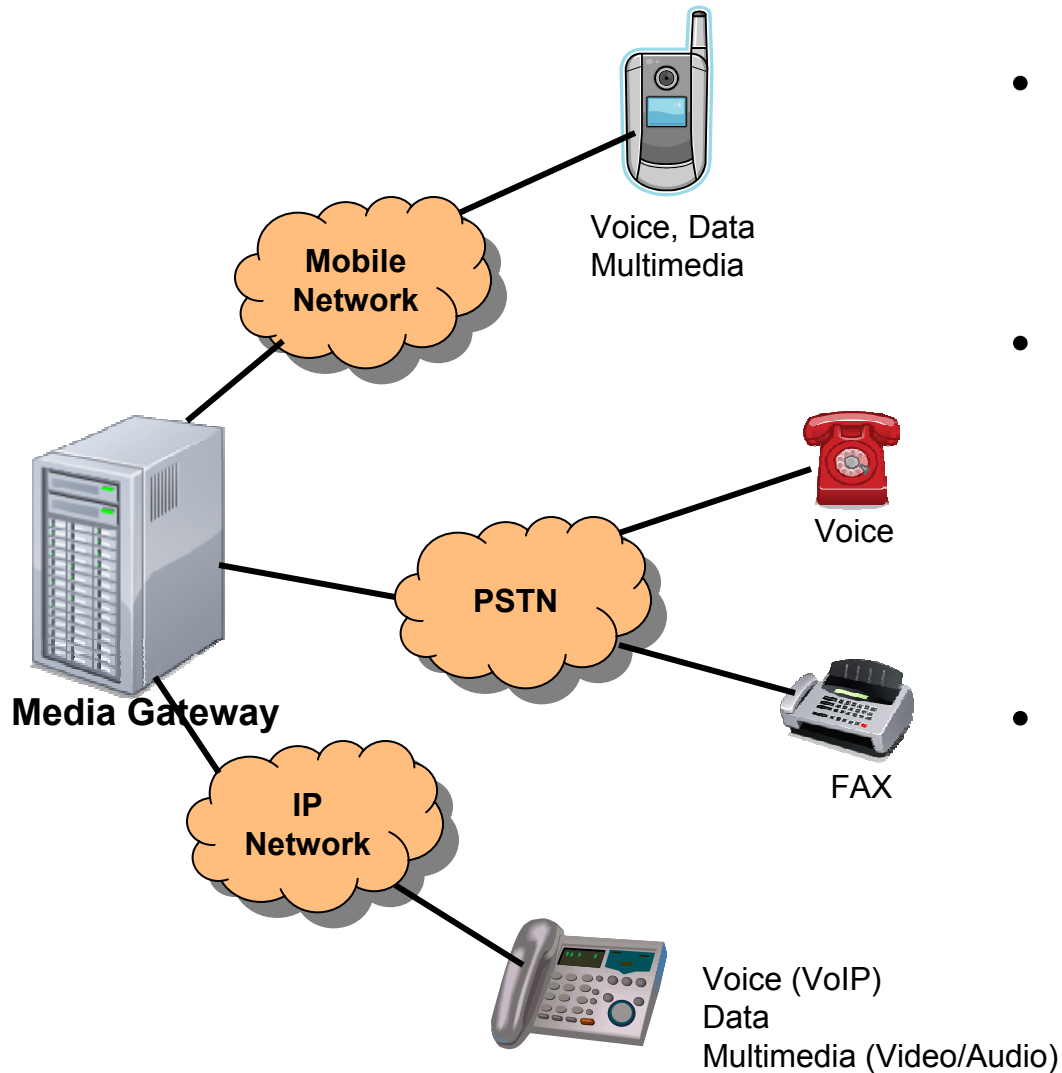


Structure

- Understanding the Complexity
 - Design Goals
 - Additional Verification Team Goals
 - Application Validation Goals
 - Environments & Tools
- Managing Complexity
 - Breaking the complexity
 - Staging it out
 - Reuse



Media Gateway



- Convergence of Fixed Line & Mobile Services
- Mobile Broadband Data - not just Voice: email, Multimedia, Streaming Multimedia, Interactive
- IP as the Pervasive Network Transport Technology

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TI Proprietary Information

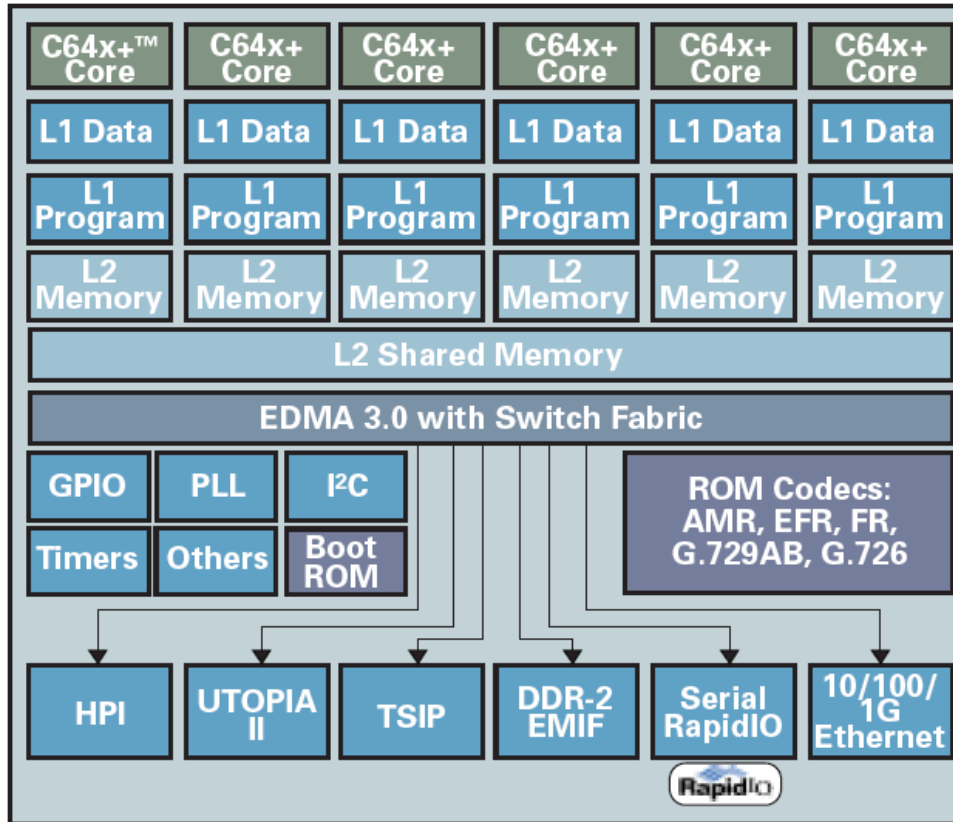


Innovation for Communications Infrastructure

Performance

Power

- Increases Channel Density by 3X
- Over 500 G.711 Channels
- Over 200 G.729 Channels
- C64x+ enables Audio/Video Transcode
- Enabled by world class software:
Telogy Voice Software Bundle, Voice & Video Codecs, Telinnovations Line Echo Cancellation Software, PIQUA Software



- 6 x 500 MHz C64x+ Cores allow performance at lower voltage
- Large Shared L2 Memory and next generation peripherals reduce system power dissipation
- Separate power domains for high performance/high power peripherals

TNETV3020



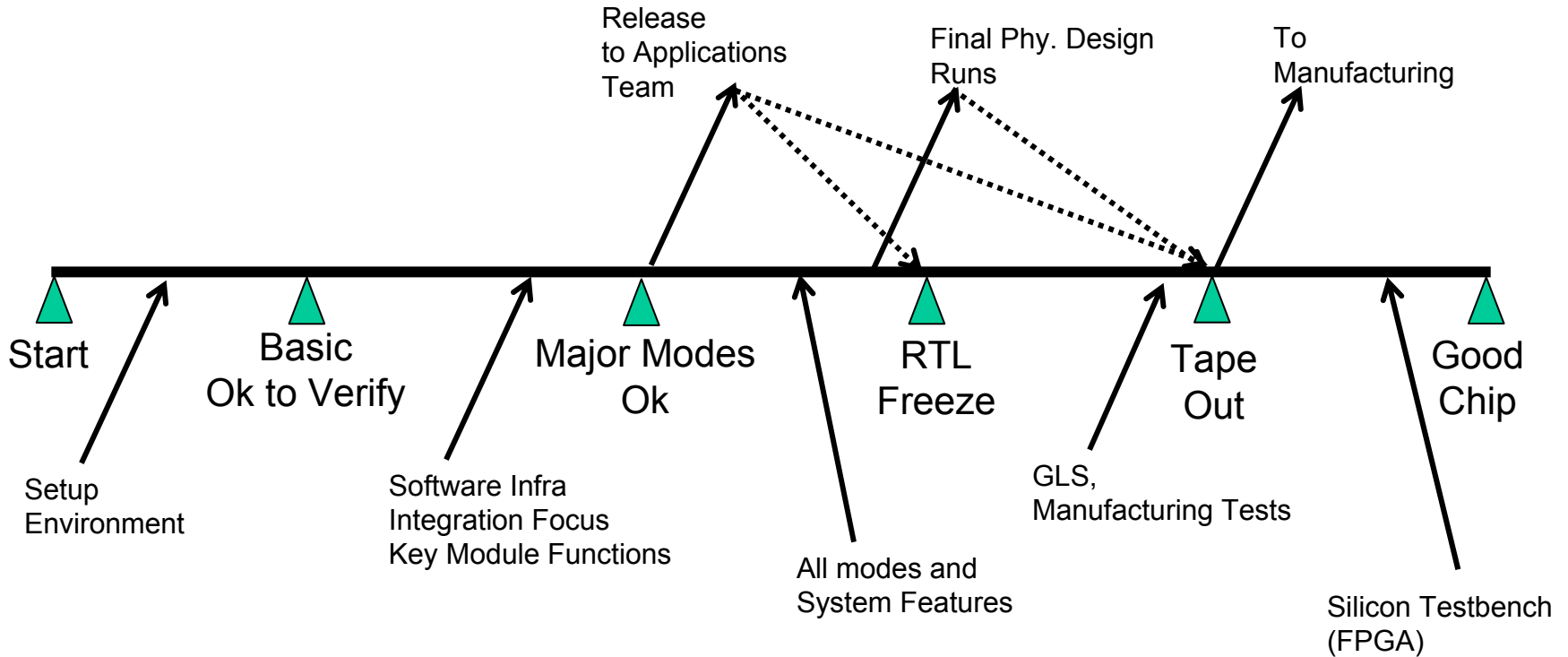
Design Complexity



- Large Design
 - 10-15 M Gate Complexity
 - Multiprocessor System - symmetric multiprocessing
 - Local and Shared Memory
- Complex High Speed Interfaces : DDR, SRIO, Gigabit Ethernet
- IP reused from previous designs + new IP developed concurrently - locally as well as by remote teams
- Power Management : Power Domains as well as Clock Gating
 - Dynamic as well as Static (some IPs always powered off or powered on)



Verification Goals

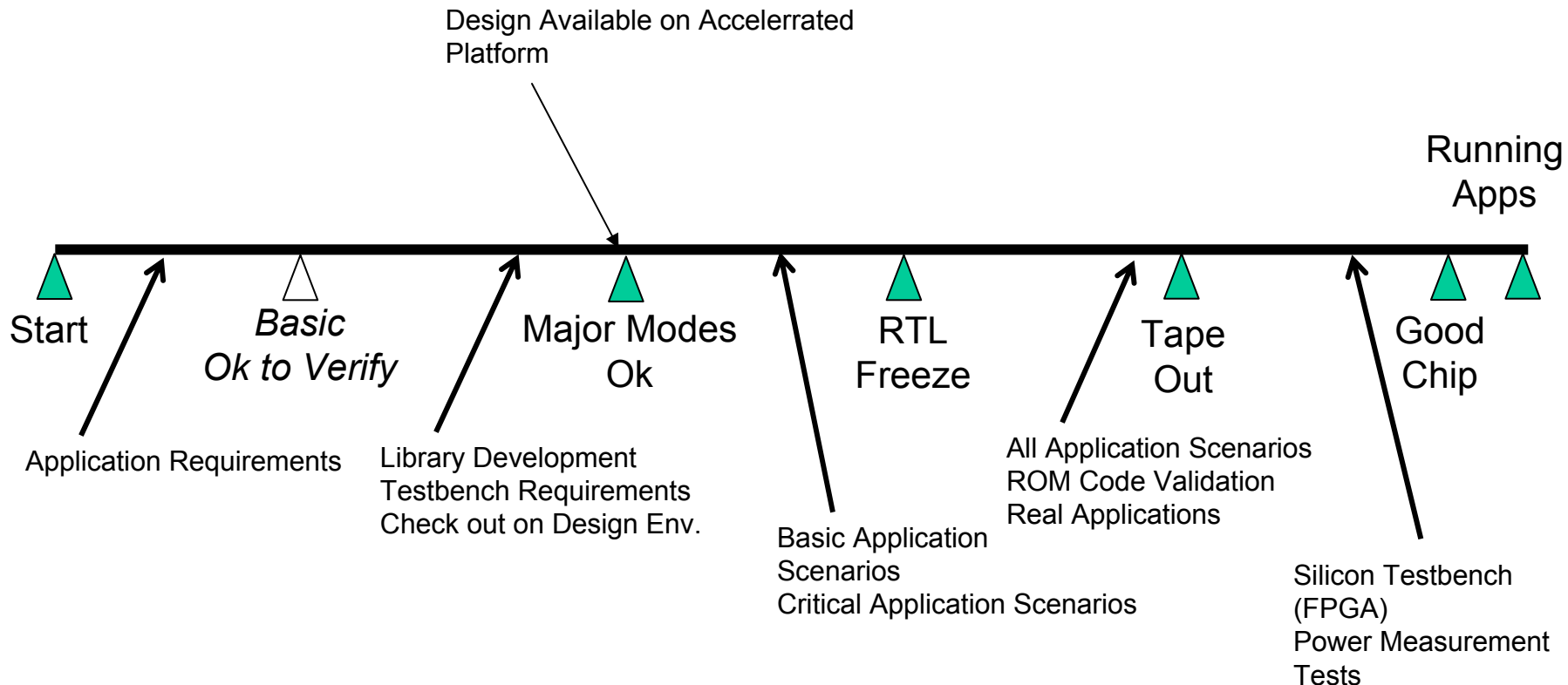


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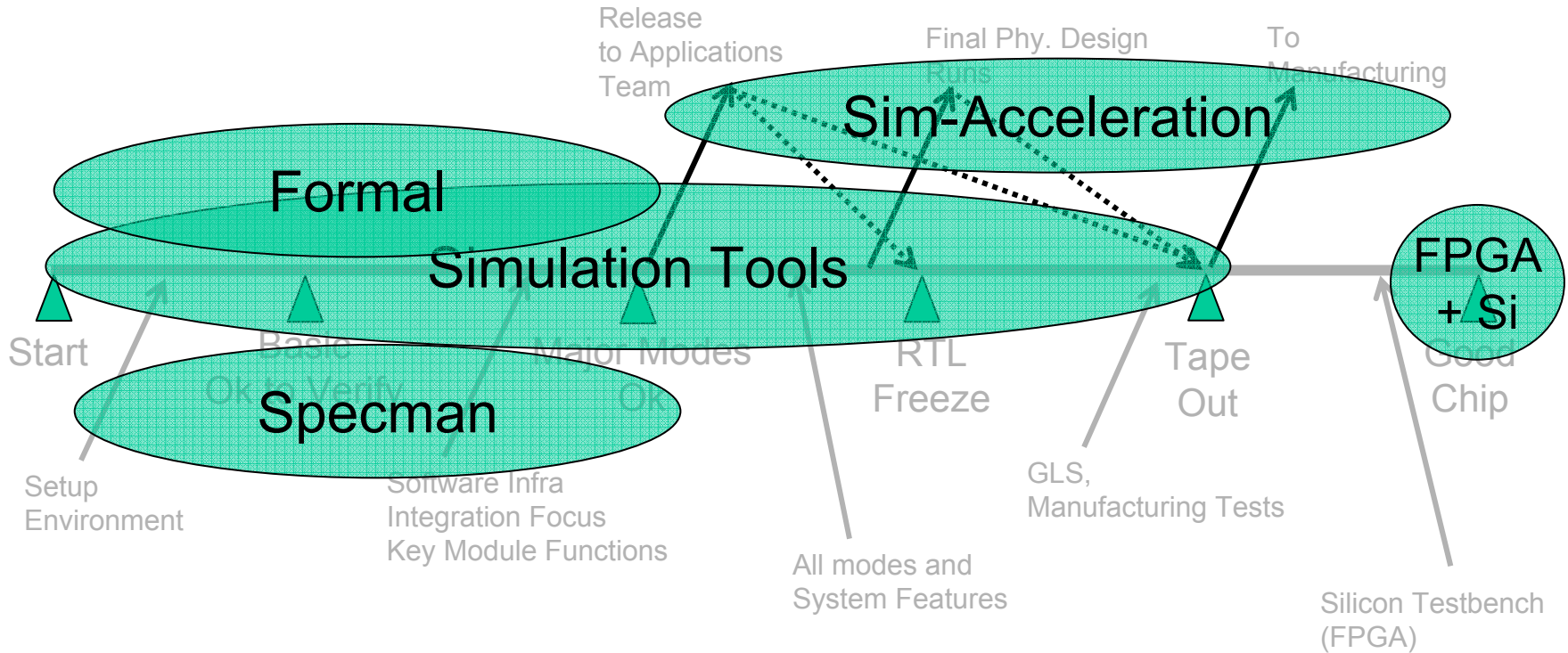


Application Validation Goals



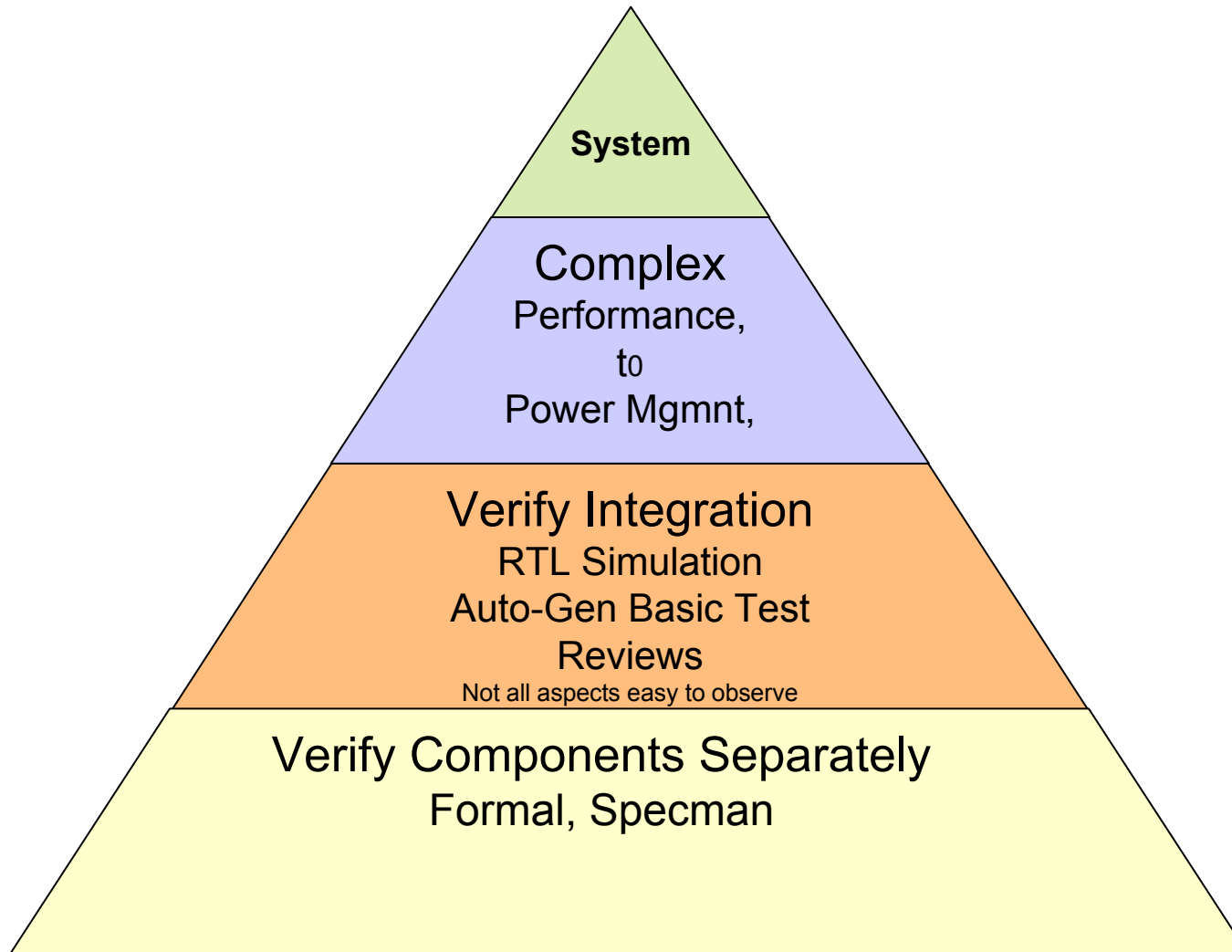


Environments





Managing Complexity



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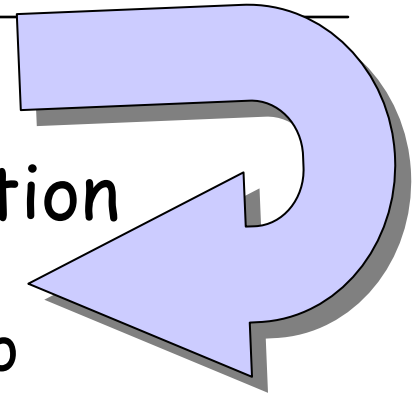
Technology for Innovators™

 **TEXAS INSTRUMENTS**



Reuse

- Same test-bench used for RTL simulations, GATE level, acceleration platforms and final Silicon
 - As Simulation Model, Synthesized to Acceleration Environment and FPGA
- Same tests can run in all environments
 - Not all are run. Actual runs are based off needs.
- Reuse test benches and tests across designs
- Share some low level and data bases code with software teams
- Use test generators for basic tests





Multiply & Not Add

X

- Break up tests into components that could be permuted
 - Same tests can be run from various memory locations and PLL configurations
 - With or without interrupts
- Tests written for one CPU run on other CPUs
- Multiple individual tests combined to run on multiple CPUs
- Simple, small tests written so that changing defines could make them large and complex tests
- Write tests like any software - build them in layers



Summary

- Verification teams not just prove designs
 - they support H/W - S/W verification too - Systems not just Chips
- Complexity broken out
- Application Validation and Design Verification use a similar environment
- Early Application Validation
 - High confidence on chip at Tape Out
 - Applications running a few days after Silicon