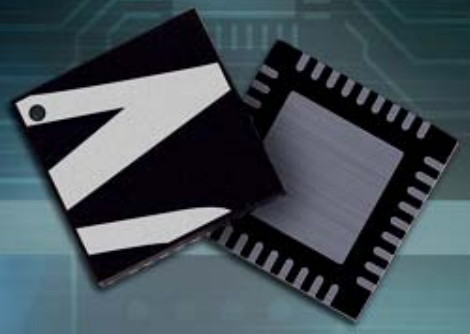
Verilog-AMS for Mixed-Signal Integrated Circuits



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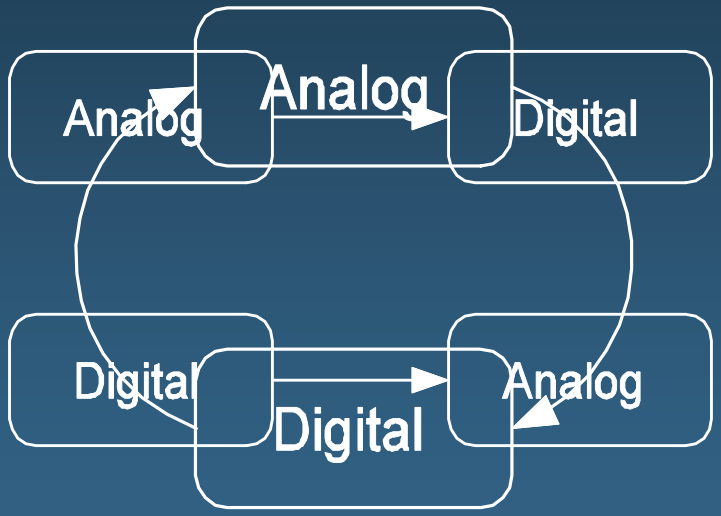
Introduction

- Integrated Circuits are increasing in Size and complexity.
- More complex interface between digital and analog makes verification difficult.



Previous Simulation Solutions

- Mixed signal simulation with two simulators
  - Complex interface elements
  - Convergence issues
  - Slow simulation
- Verilog simulation
  - Analog must be modeled as discrete with limited checking
  - No analog results
- Spice simulation
  - Need synthesized netlists
  - Very slow simulation

Verilog-AMS

- Verilog-AMS is a mixed signal language and simulation tool that can be used for mixed signal modeling and simulations.
- Benefits of using Verilog-AMS
  - Simplification of modeling mixed signal circuits
  - Possible to greatly decrease simulation time
  - Mixed signal verification
  - Architecture design and validation

Modeling Improvements

- Verilog-AMS uses most constructs from Verilog and Verilog-A languages
  - Analog and digital content can be contained in one model
- Signals can be declared as “logic” or “electrical”
  - This allows for a model to have both digital and analog I/O
  - If done correctly, no connect modules or interface elements will be needed

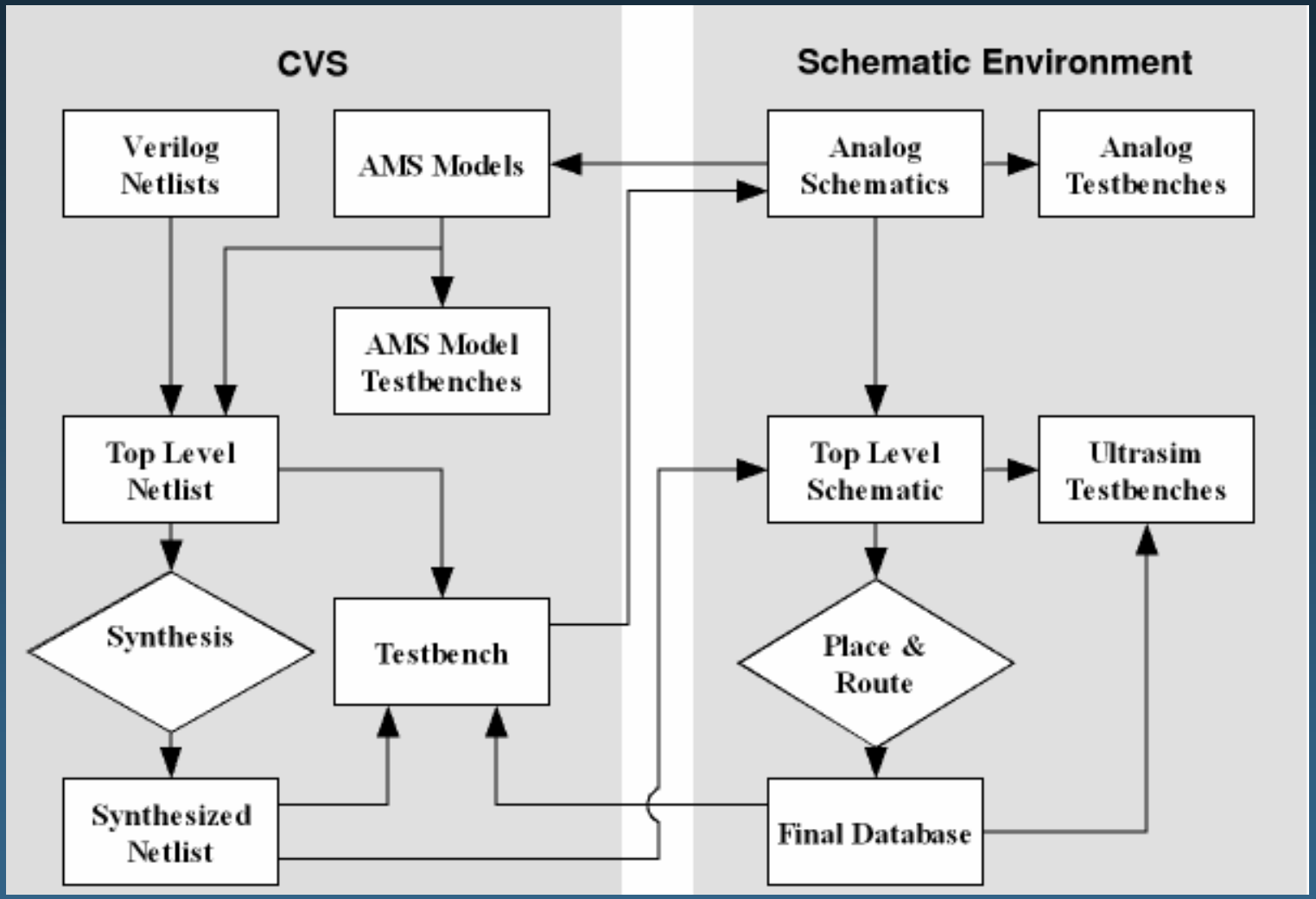
Modeling Necessities

- Polarity of I/O and dependency on control signals
- Dependency on analog signals (power, biases, etc).
- Timing
- Bandwidth, Slew rate, and Voltage limits of analog signals

Special Model Considerations

- Some models may be created with a fast/ accurate option
- Hierarchy of circuits should match physical placement
  - All pin names and directions the same as the schematics
  - Same circuit name to be easily imported
- Matching of signal types!!
  - Important for simulation time

Zilker Labs Design Flow



Successes

- CVS use of netlists and models
- No problems with analog/digital interfaces due to polarity mismatch or timing issues
- Less chance for miscommunication in the conveying the operation of the circuits
- Fast simulation at the top level
  - More circuit functionality verified before tape-out
  - Standard testbenches with pass/ fail outputs for regression testing
- System level simulation
- Functional samples at 1st Silicon

Areas of Improvement

- Incorporate models into schematic environment
  - Allows for common testbenches
  - Better verification of model accuracy
- Architecture level modeling using Verilog-AMS

Conclusion

- Verilog-AMS can greatly improve design cycles by
  - Increasing verification of digital to analog interface at the top level of the design
  - Significantly reducing the top level simulation time.
  - Determining appropriate analog specifications for analog circuits.
  - Creating an appropriate environment for chip architecture design.