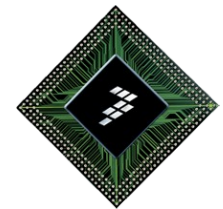


Verification of the QorIQ™ Communication Platform Containing CoreNet™ Fabric with SystemVerilog

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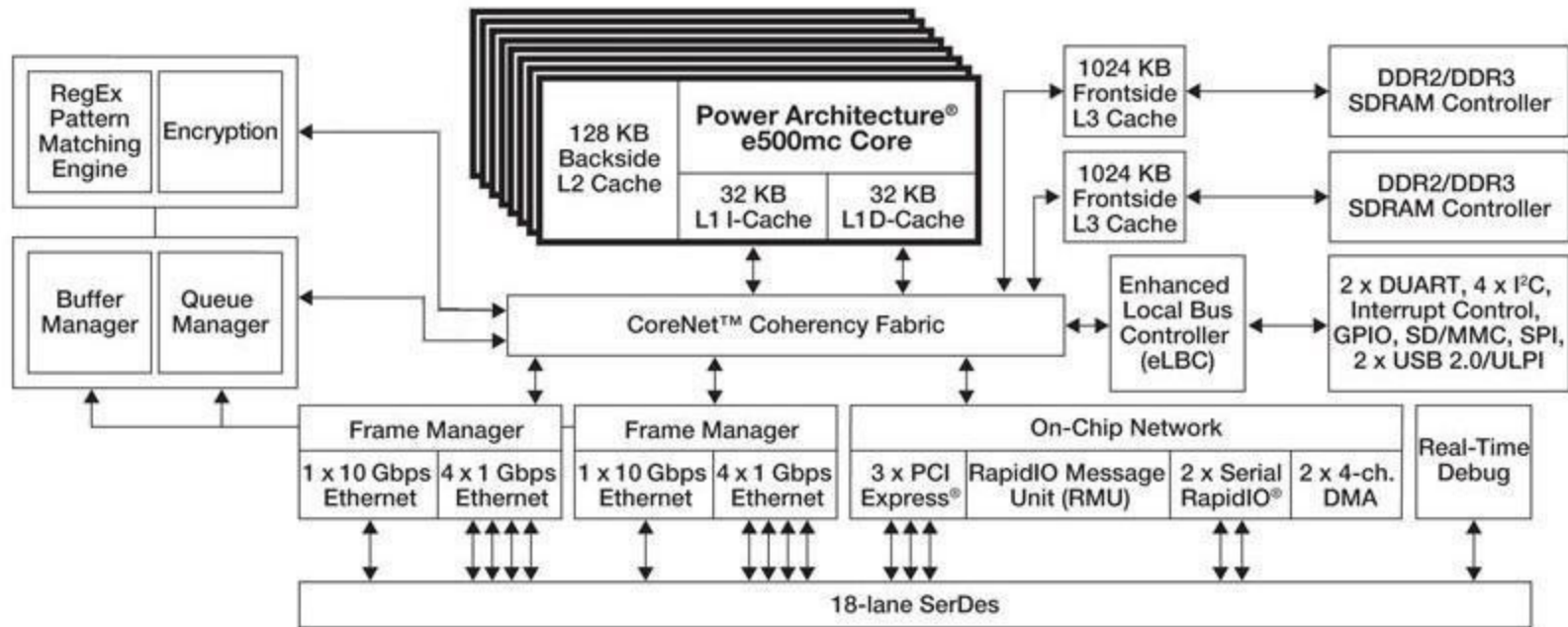


- ❖ Introduction
- ❖ Verification Challenges
- ❖ Verification Methodology
- ❖ Verification IP
- ❖ Conclusions
- ❖ Q & A

- QorIQ™ (***pronounced*** 'core eye-queue') Overview
 - Communication Processors for networking applications
 - Multi-core with tri-level cache hierarchy
 - Intended for combined control, data-path and application layer processing
 - Freescale processors based on Power Architecture ®(PA) technology
 - New CoreNet™ Interconnect on-chip fabric

QorIQ P4080 Communication Processor

QorIQ™ P4080 Block Diagram

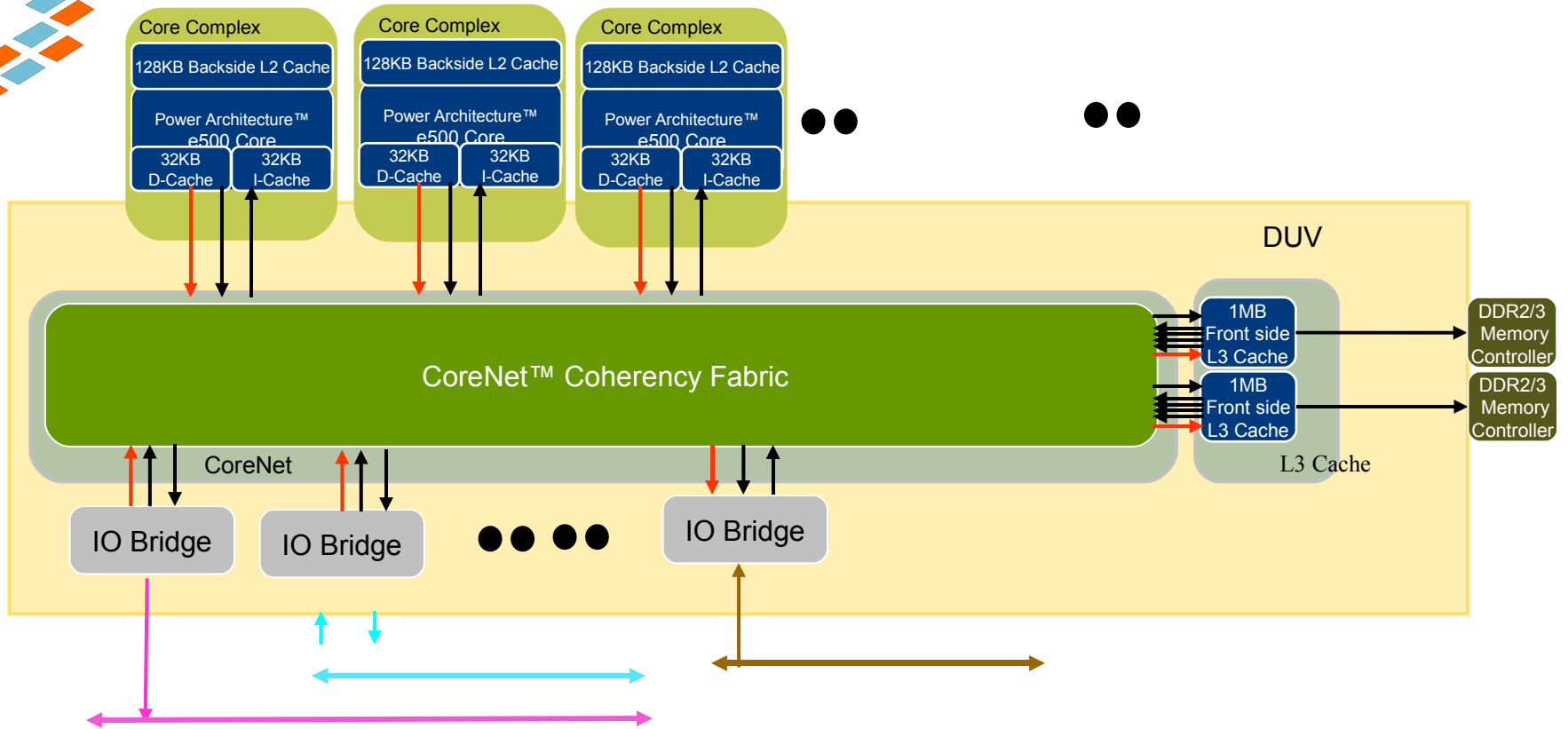


■ Cores

CoreNet™ Platform Overview

- CoreNet fabric sub-system is referred to as CoreNet Platform
- CoreNet is an on-chip, high efficiency, high performance multiprocessor coherent interconnect
- Point-to-point interconnect
- Independent address and data paths
- Pipelined address bus, split transactions, out-of-order completion
-

CoreNet Platform Block Diagram



- ❖ QorIQ & CoreNet Platform Overview
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Verification Challenges

- Multiple and new architectures to verify – CoreNet, Arbitration, Address Map, Security, Virtualization etc.
- Extensive VIP development to support unit verification
- New constrained random stimulus and associated coverage
- Performance
- Parameterized design to support multiple derivatives
- Deal with legacy VIP
- Adoption of new languages and tools (SV, SVA)

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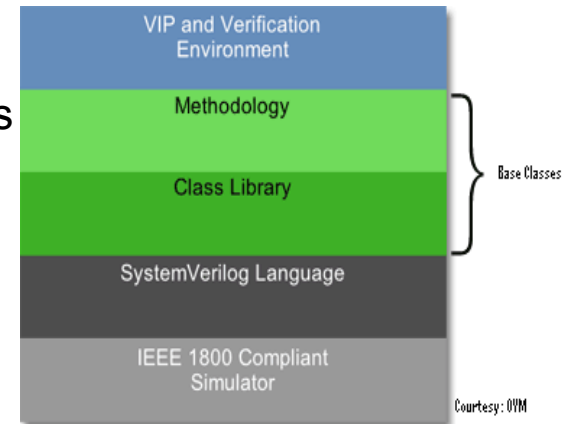
Verification Methodology

- Top-down – black box to white box
- Transaction Based Verification Methodology (TBVM)
- Coverage driven
- Extensive correctness checking
- Hierarchical Verification
- Reuse, reuse, reuse!

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SystemVerilog Testbench

- **SystemVerilog Base Class Library (SVBCL)**
 - Basic building blocks for constructing testbenches
 - Same concept as OVM or VMM libraries
- **SVBCL Extensions**
 - Register randomization, randomization routines
 - Algorithmic and random stimulus base classes
 - Enhanced run-time parameter management
 - Address manager to manage address regions between masters
 - Data manager for intermediate and final results checking
 - Cache/Memory preloaders and checkers
- **Platform Verification IP**
 - Extensive set of BFMs for CoreNet and all other IP protocols
 - Monitors, Assertions, Coverage
 - Random and directed stimulus



CoreNet VIP Overview

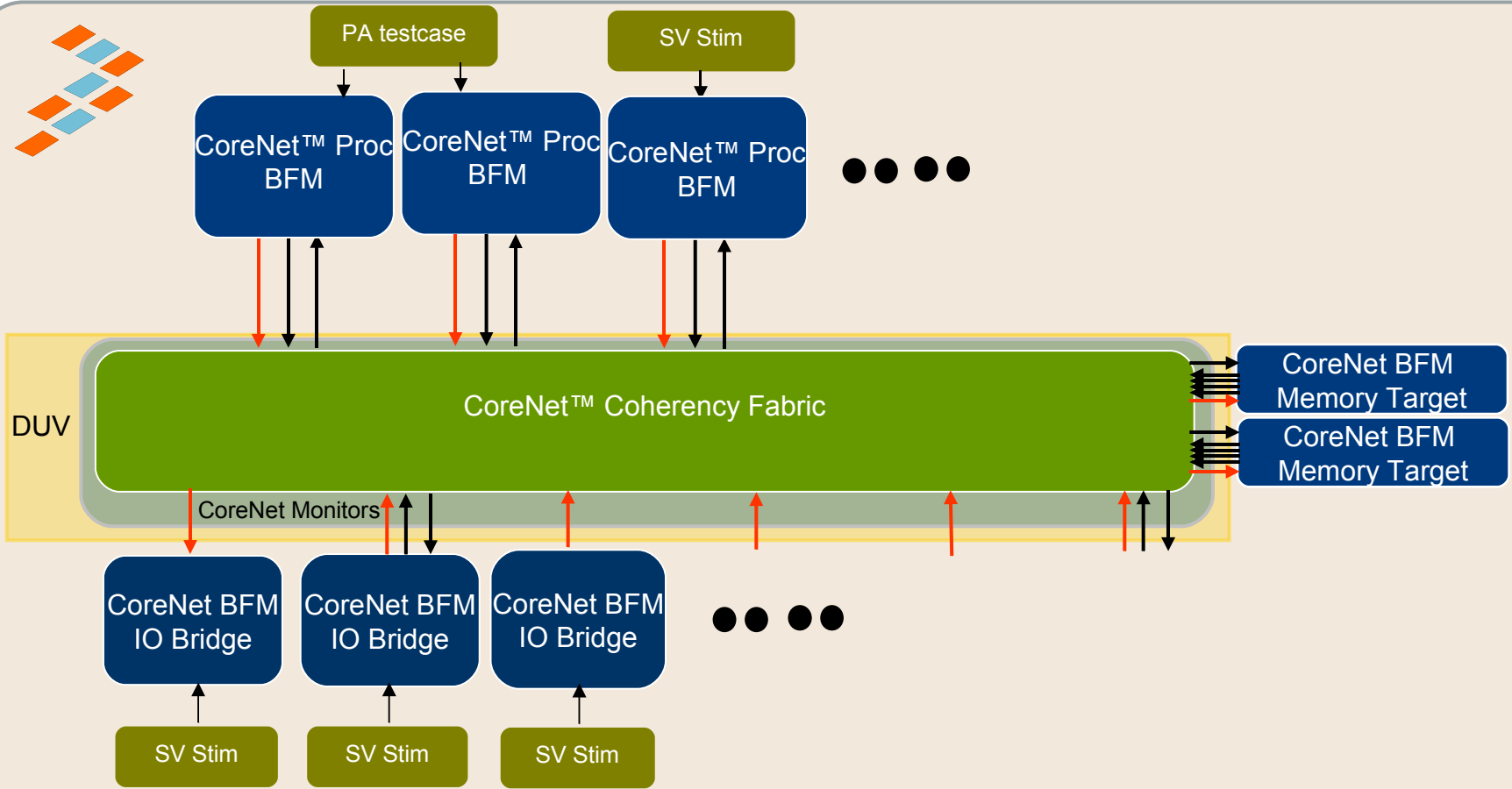
- Object oriented model of all platform CoreNet-compliant units – Fabric, Proc Master, IO Bridges, Targets.
- Includes BFM, monitors, coverage and stimulus objects
- Layered Architecture of BFMs
 - Stimulus Layer - higher level stimulus objects
 - Transaction Layer – implements transaction attributes of CoreNet
 - Link Layer – implements flow control aspects of CoreNet
 - Phy Layer – implements physical attributes of CoreNet protocol
- BFMs model buffer resources, significant towards finding deadlock issues
- Embedded coverage using SV covergroups
- Multitude of control parameters (run-time) to modify behavior at run-time

How SV helped

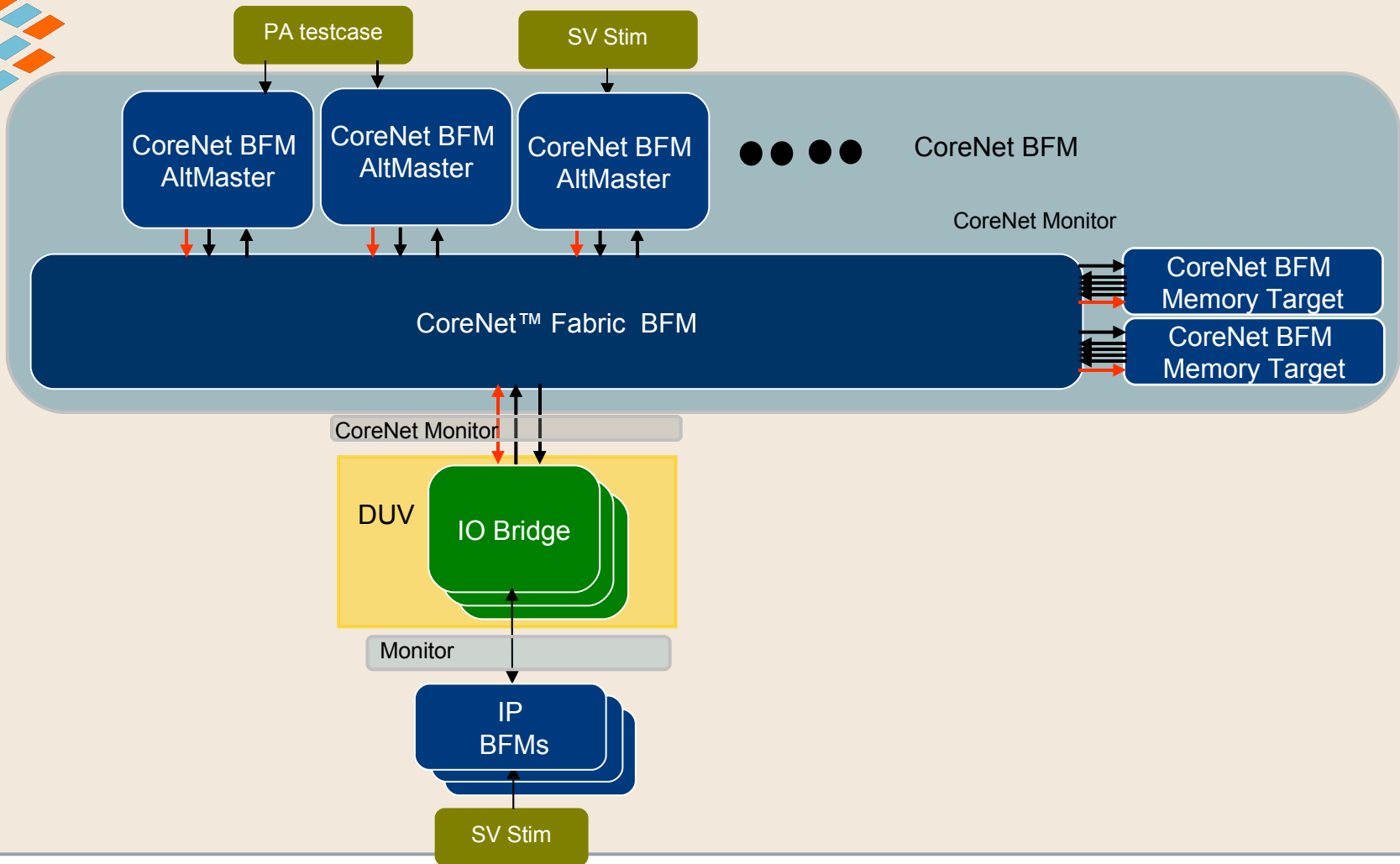
- OOP concepts – Abstraction, Inheritance & Polymorphism
- Object-based randomization and constraints programming
- Enhanced inter-process synchronization and communication mechanisms
- Fine grain process control (fork...join)
- No memory leaks (automatic garbage collection)
- Enhanced tasks and functions
- Interfaces (parameterized, nested)
- Powerful assertions & functional coverage capabilities

- Constraint-solving
- Unsupported constructs (e.g. parameterized classes)

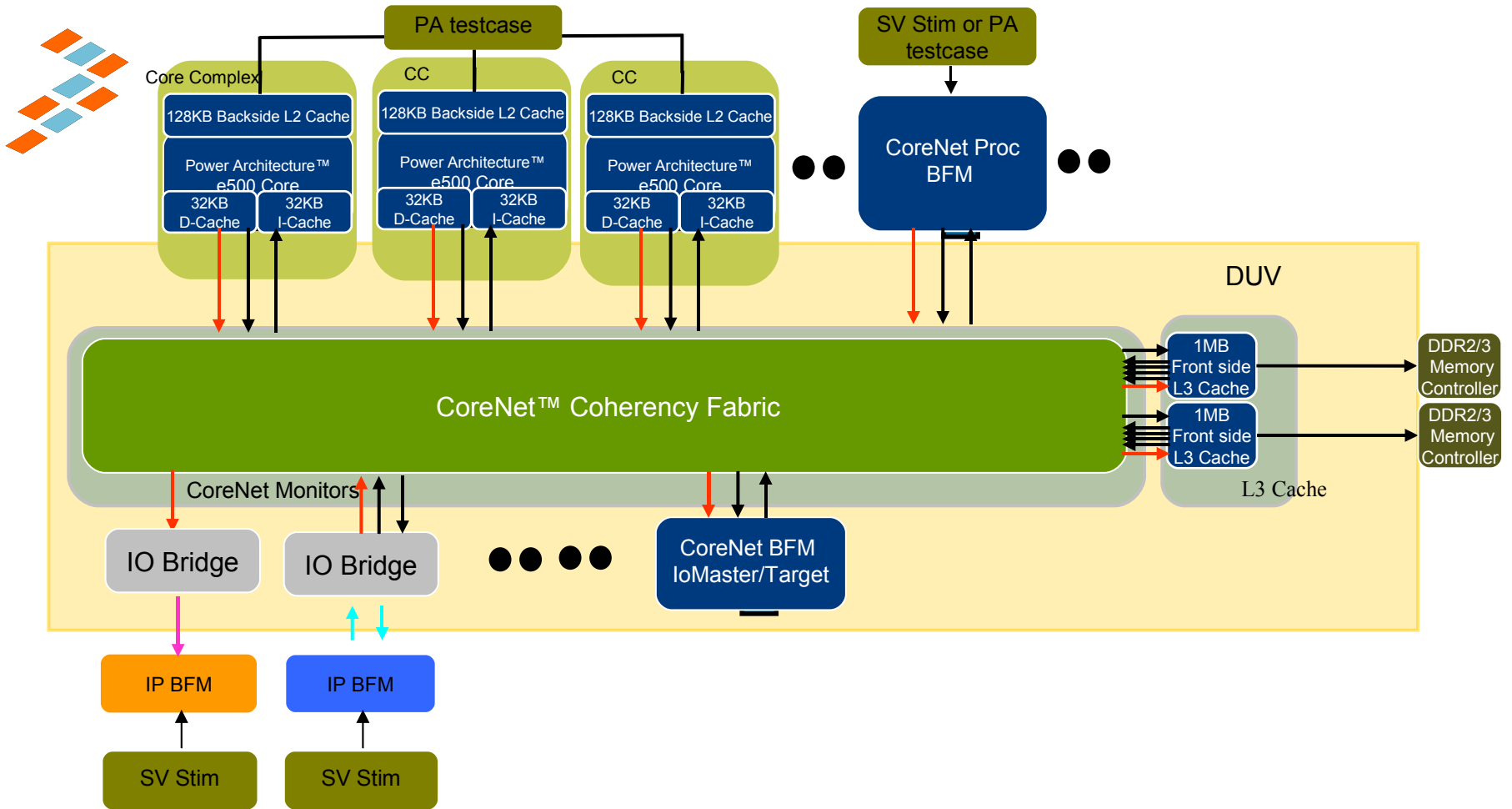
Corenet Fabric Testbench



IO Bridge Testbench



CoreNet Platform Testbench



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Successes

- Successfully verified the entire CoreNet platform as an early adopter of System Verilog for testbenches.
- Successfully applied advanced features of SV in creating a lean and efficient testbench with focus on reuse.
- Reuse of CoreNet VIP for verification by cross-functional and cross-site teams.
- Feature-rich testbench enabled early performance verification on RTL - helped flush out many performance bugs

continued...

Successes

- First Networking & Multimedia Group (NMG) SoC with fully integrated SV testbench
- Sampled first silicon to customer in less than 3 weeks!
- Customer is able to run 8-way MP software.
- No major (show-stopper) functional CoreNet bugs in silicon
- Lab Bugs/Verif Bugs = 0.7%
- Found SV to be adequate for verifying complex designs.

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