# Wireless
# Low Power and Verification Challenges

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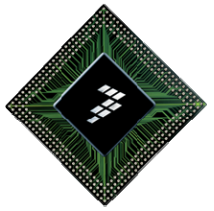

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# Wireless Carriers

Low Power Design is business critical need and has a direct impact to carrier revenue.

**If the cell phone is powered off, The source of revenue is off for carrier.**

**Performance needed to sell the phone. Power needed to bring revenues.**

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# Wireless and Handheld Devices

- ►Standby & Talk time - Benchmark parameters in cell phone industry.
- ►Music playback time - Benchmark for MP3 capable phones.
- ►Frequent battery charging - Major negative in consumer mind.
- ►Increase performance with large battery – Increased Cost
- ►Increased Heat in phone – Increased liability and TCO.

❖Power Performance ratio must be very high to win consumer mind.

End Consumers are becoming power aware and can make intelligent decisions and smart choices on power.

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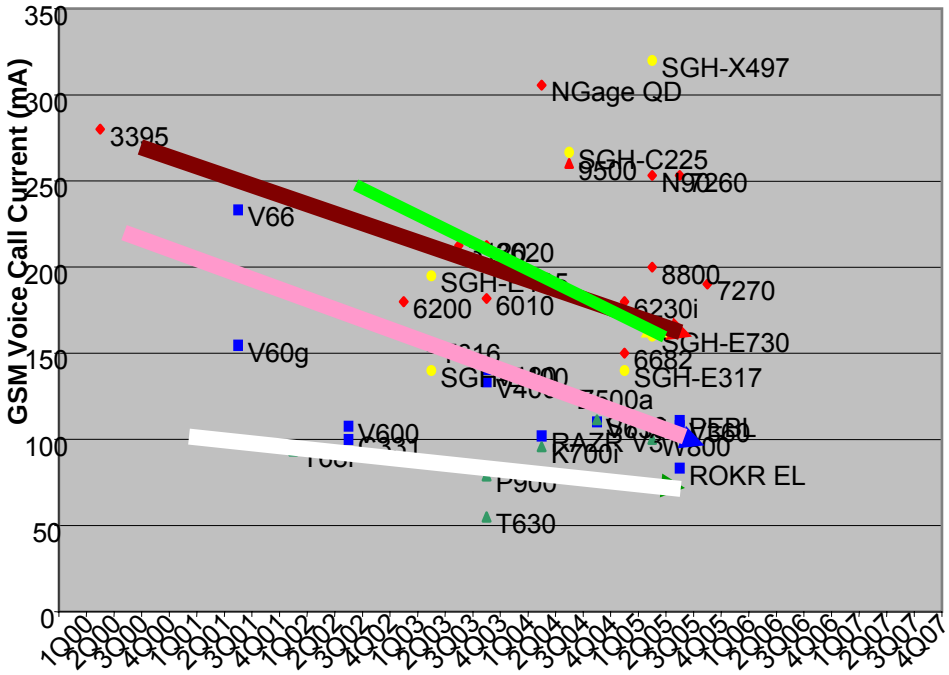
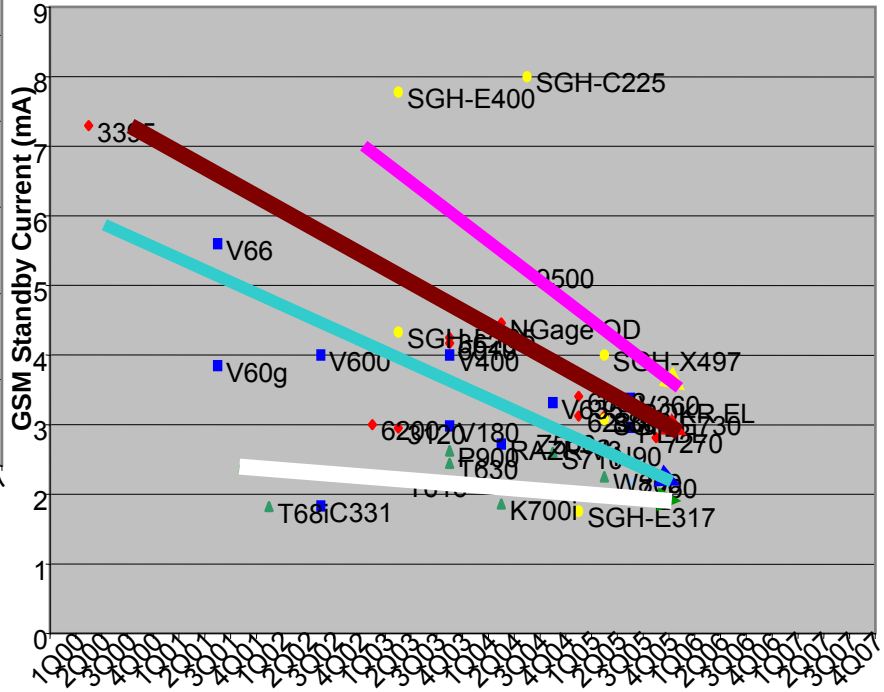
# Trends - GSM Phone Current




GSM Talk Current




GSM Standby Current

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# Leakage Current in 65nm, Major concern for Wireless Design

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# It’s about Energy

## Goal: Extend Phone Battery Life

- Battery life is proportional to energy consumed
- Energy is power consumed over time
- Wireless designers must manage energy consumption.

To extend battery life, designers must minimize active and leakage power.

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# Problem Focus View

| | |
|---|---|
| **Design Intent** | **Hardware support for power gating, low-power idle modes, SRPG, AWB, DVFS, DPTC, Biasing techniques at all levels.** |
| **Design Implementation** | **RTL2gds, Power Integrity, Multimode synthesis, Placement, power grid creation, analysis, power estimation** |
| **Design Verification** | **Behavioral and RTL verification, Gate level verification, testbench styles, static and dynamic power Rule checking.** |
| **Low Power infrastructure** | **Support library infrastructure with special cells. New cells and parameters for cz. Multimode/multivoltage support infrastructure.** |
| **PROCESS node Definitions** | **Transistor design, Vt Optimization, memory bitcell design. custom and reusable analog. Silicon correlation.** |

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# Low Power Design Needs

►Support Low Power Design Techniques thru the entire design flow using a single file format.

- Design Representation
  - Accurately define and capture the low power design intent, modes and constraints.
- Design Implementation
  - Floorplan and power grids.
  - Common constraints for all tools (Synthesis, APR, timing, DFT)
  - Design analysis tools with single power constraints.
  - Accurate power estimation and measurements
- Design Verification
  - Voltage oriented simulators
  - Various static power technique modeling and simulations.
  - Silicon validation and correlation.

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# Static Power Design

- Static Power is crucial for defining standby time of cell phone.
- Multiple Leakage Reduction Techniques
  - Active Well Biasing (AWB)
  - State Retention Power Gating (SRPG)
  - Save and Restore with power gating. (S&R PG)
  - Multi-Vt based design styles
  - Aggressive Voltage Reduction during standby mode (RV)
  - Device  biasing.
  - Switches, Isolation collars and level shifters.
- Static Power a big part of active power
  - Use switches for power mode switching.
  - Thermal dissipation issues in packaging.

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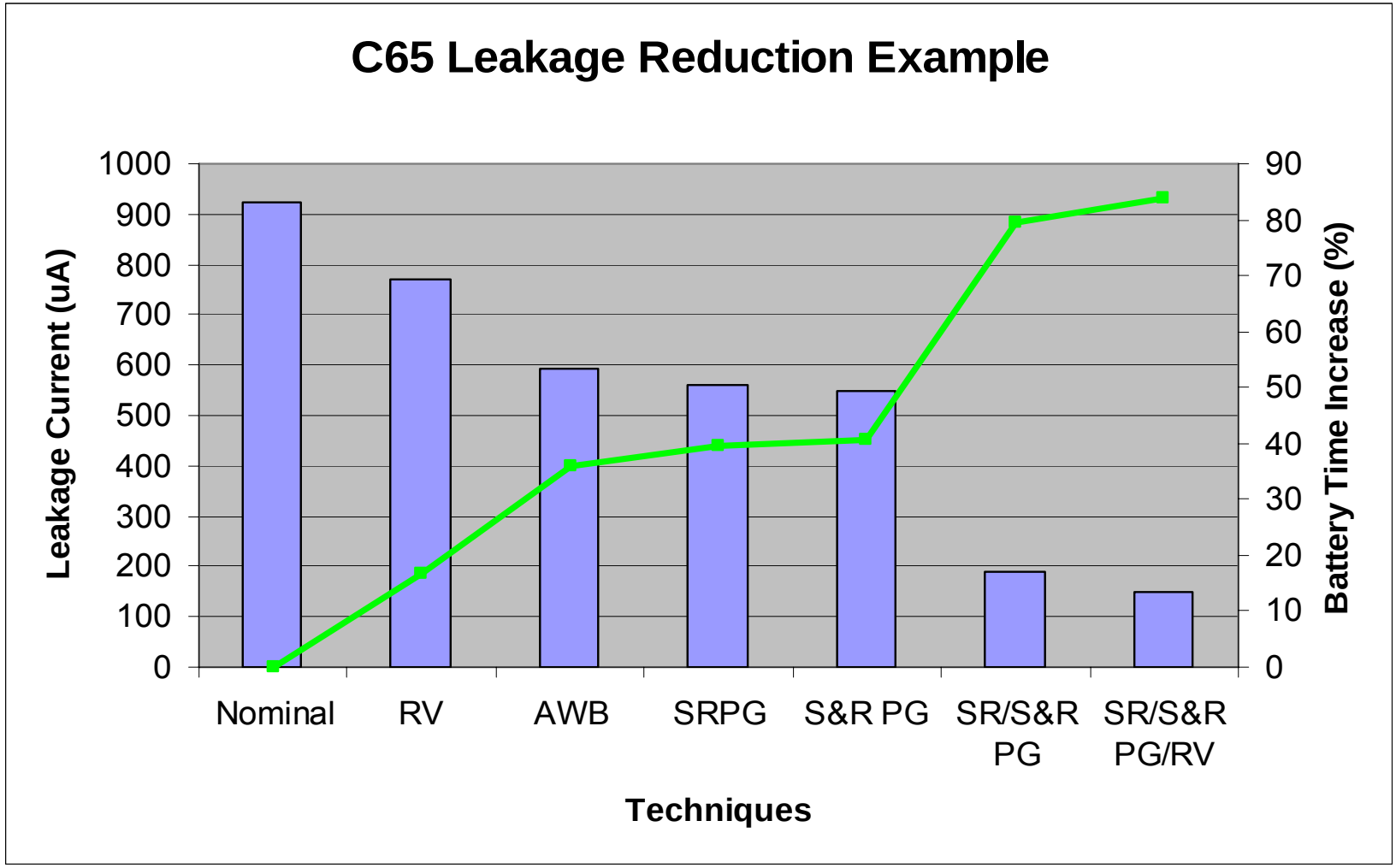
# Example Leakage Reduction Techniques

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# Multi Voltage Design Styles - DVFS

►Voltage has quadratic effect on power.
►In Multivoltage design Style
- Unused portion of design is switched off.
- Low performance portion is running at lower voltage
- High performance portion is at higher voltage.

►Voltage partitioning decisions are crucial and very key for power performance factor.
►Clocking is the major challenge for multivoltage designs. Need intelligent clock tree builders.
►Asynchronous protocols to enable efficient voltage partitioning.
►Design is optimized for multi voltage conditions.

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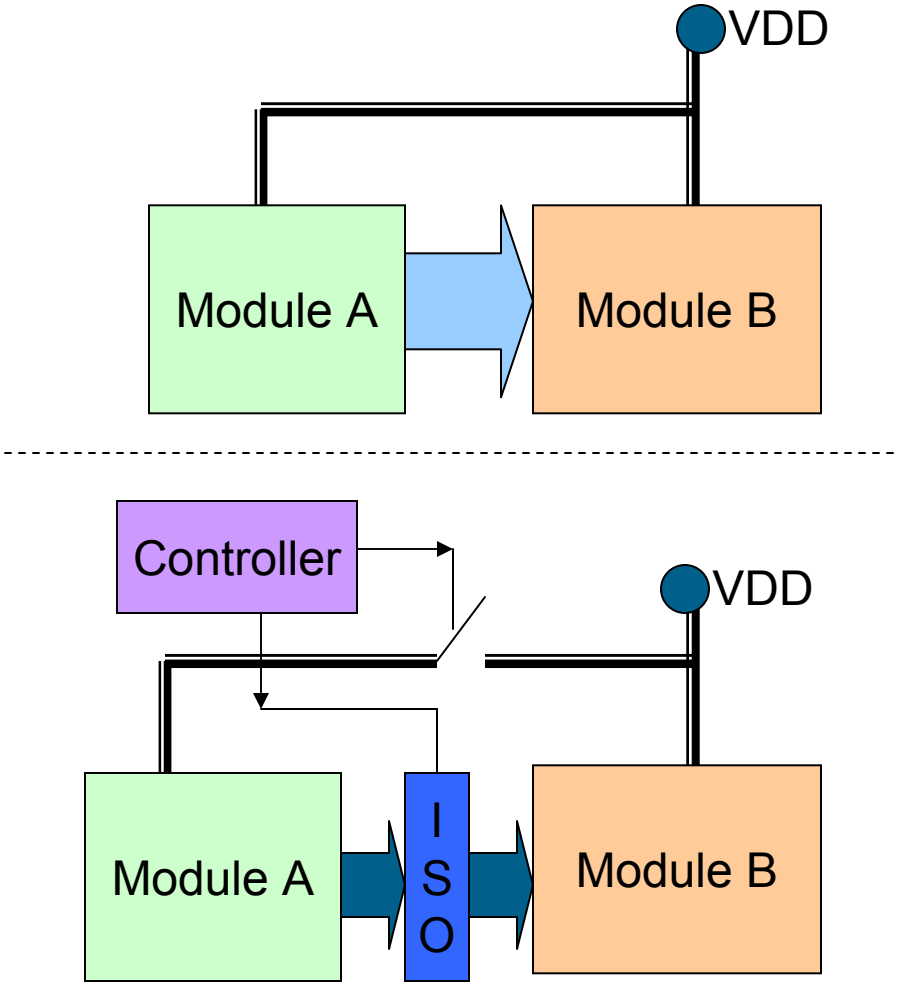
# Isolation and Percolation

- ►Picture power managed vs non power managed design implementation
- ►When a module is powered off, outputs will float.
- ►These outputs can corrupt the state of receiving modules.
- ►Modules must be isolated
- ►A separate logic is inserted to isolate and percolate.
- ► Logic State of isolation is important and can cause adverse effects if improper.

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# Retention Verification

►A module can be turned off to save leakage.

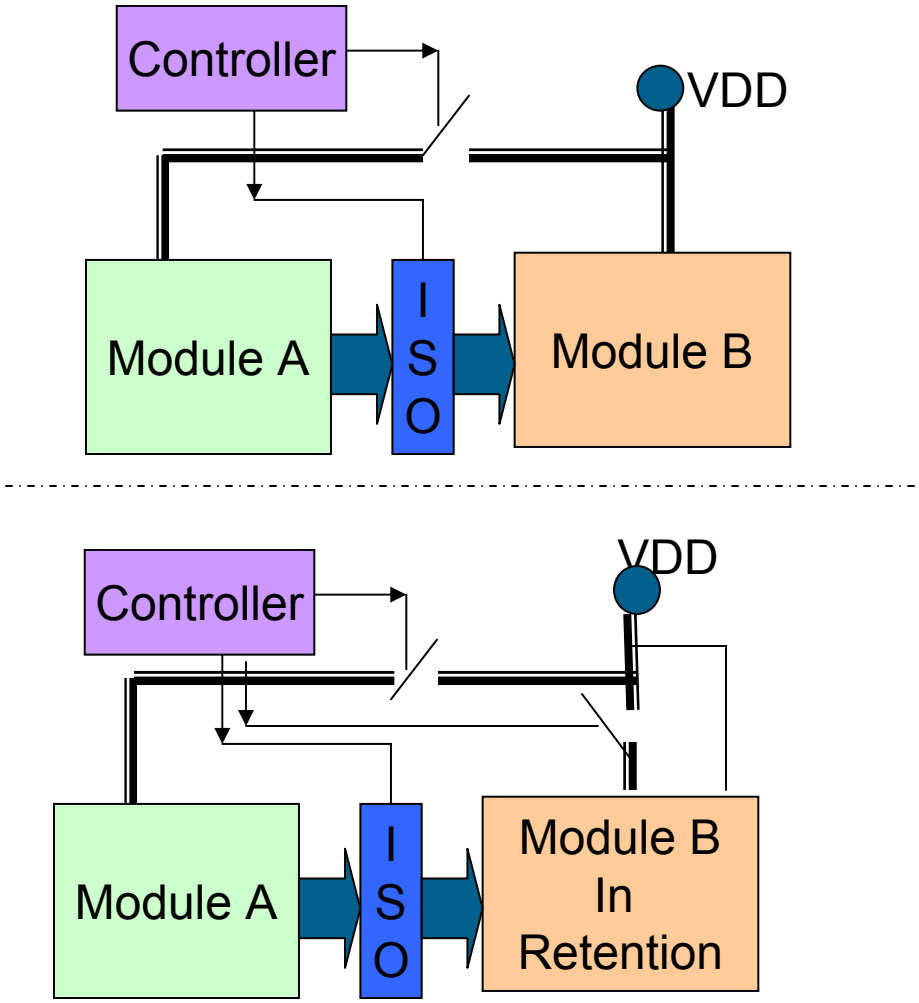
►The state of module B must be retained during power off.

►Special circuits and flipflops have been created for this purpose.

►Need to verify

- The state was saved correctly.
- State restored correctly.
- System can function after powerup.

►The controller must ensure the correct save and restore sequence.

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# Voltage and Frequency Variation

►Voltage of module A is reduced when lower performance need.

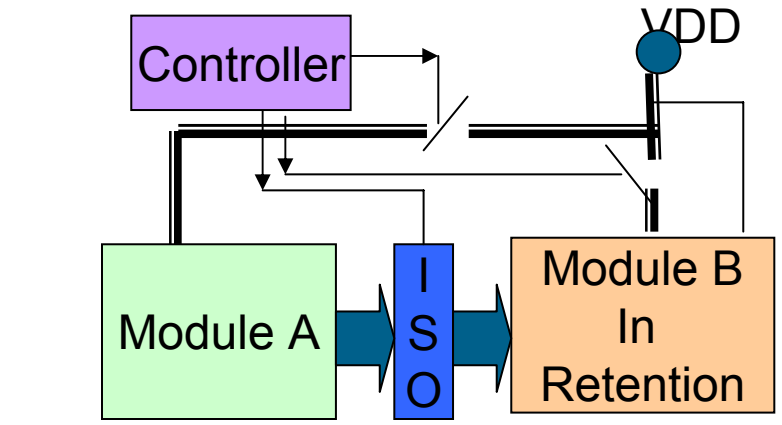
►Change of voltage is associated to change of Clock.

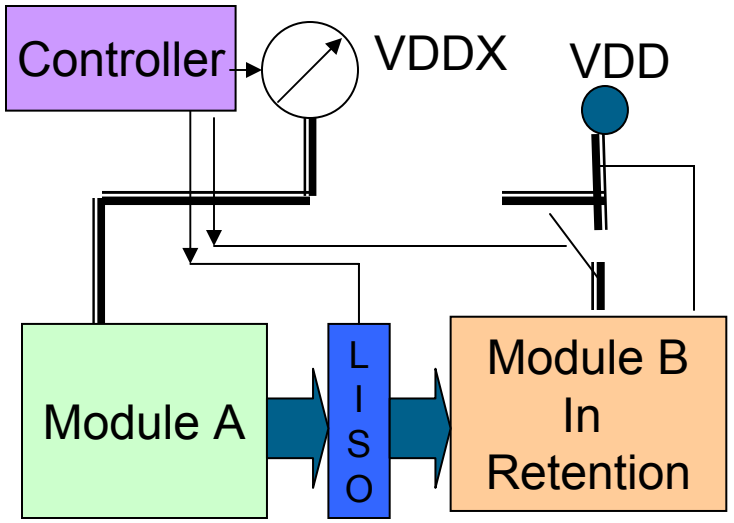
►Isolation is now Lisolator. (level Shifter & isolation)

►Need to verify

- System performance state.
- Prepare & communicate regarding voltage change..
- System operational during change.
- System operational after change.

►The controller must ensure the correct operating sequence and monitor progress.

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# Power Architecture Verification

- Architectural analysis required to achieve efficient voltage partition.

- Global Power Controller
  - Partial or full power up and power down is a controlled sequence.
  - Verify the sequence control and state machine completely.
  - The Global Power Controller should be capable of capturing and relinquishing the controls appropriately.

- The system should be functional and must be verified
  - During power off process
  - After power off has completed
  - Power up decision making
  - During power up
  - Full recovery after power-up.

- Ensure consistency of Power Programming Model in specification.

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# How Does the world of Verification Change

►Verilog does not have a concept of power on/off.
►Verilog does not have association of voltage levels.
►Power shut off and multi voltage design style has brought in multiple new components in chip.
►Gate level and circuit level simulations are expensive and time consuming and very late to fix the problems.
►Functional coverage of state of system at the time of power off and activities following power up should be gathered
►All power related features must be checked at RTL stage.
►Power Equivalency Checks needed between RTL & gate.
►Power estimation in various functional mode needs to be integrated with power verification.

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