

# HW Emulators: Does it belong in your Verification tool chest?

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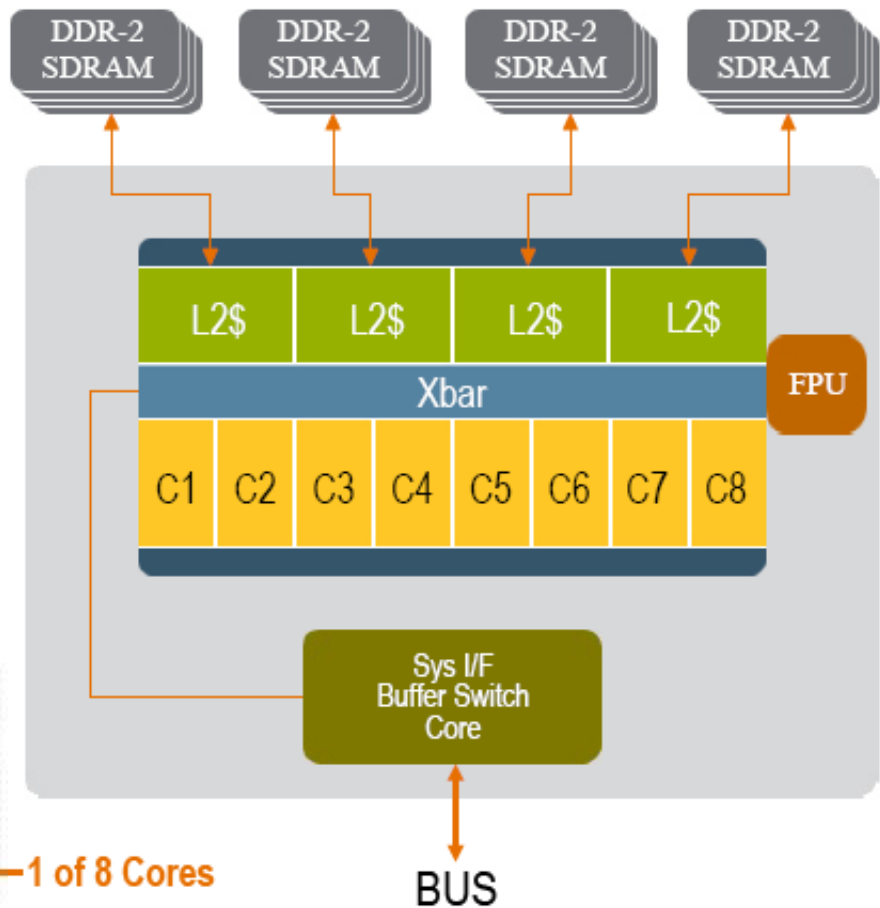
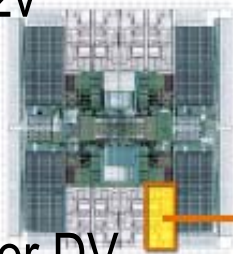
<http://sun.com>

# Verification Challenges

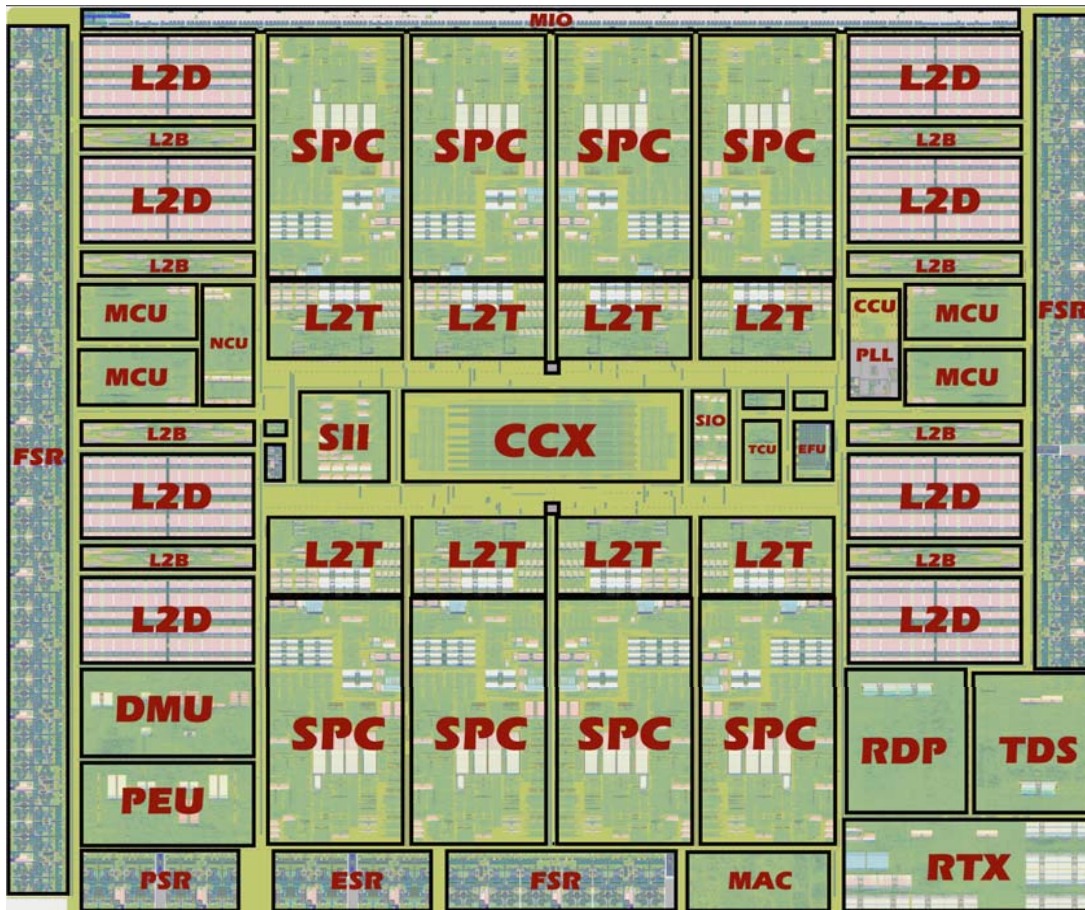
- Large SoCs -
  - > Multi-core, multi-thread every where
  - > Complex IOs: ENET, PCIE, etc.
  - > Verification state-space explosion
- Fierce Competition -
  - > Time-to-Market
  - > Cost
- Tools not keeping the pace with requirements -
  - > Capacity
  - > Performance

# UltraSPARC T1 Processor

- A true revolutionary processor
- Up to eight 4-way multithreaded cores for up to 32 simultaneous threads
- All cores connected through a 134.4GB/s crossbar switch
- High-bandwidth 12-way associative
- 4 DDR2 channels (23GB/s)
- Power : 63W @1.2GHz, 1.2v
- ~300M transistors
- 378 sq. mm die
- Verification covered in earlier DV Club presentation



# UltraSPARC T2 Processor



- True SoC
- 8 SPARC Cores, 8 threads each
- Shared 4MB L2 8-banks, 16-way associative
- 4 dual-channel FBDIMM memory controllers
- 2 1/10 Gb ENET ports w/ onboard packet classification and filtering
- 1 PCIE x8 1.0 port

# What is an Accelerator/Emulator?

- Emulation- synonymous with HW Acceleration; subtle difference – involves target system hw
- High-level proto-typing system – virtual silicon
- RTL is synthesized to gates; gates are mapped to FPGA or custom-processor based HW to execute design in parallel at hw speed
- Ease-of-use – make it appear as a fast “simulator” - more than 10,000X faster than SW Simulator

# Convince it is the right thing to do...



Emulator HW



Gulfstream jet

# Cost of Bugs – simple analysis

- Showstopper bug early in design phase
  - > Cost: almost negligible
- Showstopper bug close to tapeout
  - > Cost: schedule impact
- Showstopper bug after tapeout
  - > Cost: Few Silicon respins, schedule impact
- Showstopper bug close at Revenue Release
  - > Loss of Revenue at \$1+ Million per day
  - > Reduce competitive edge
- Showstopper bug 1 year after Revenue Release
  - > Cost of recall at \$150Million
  - > Damages corporate reputation

Source: N.Winkworth & B.Blohm

**Getting SW/HW right the first time is critical to survival!**

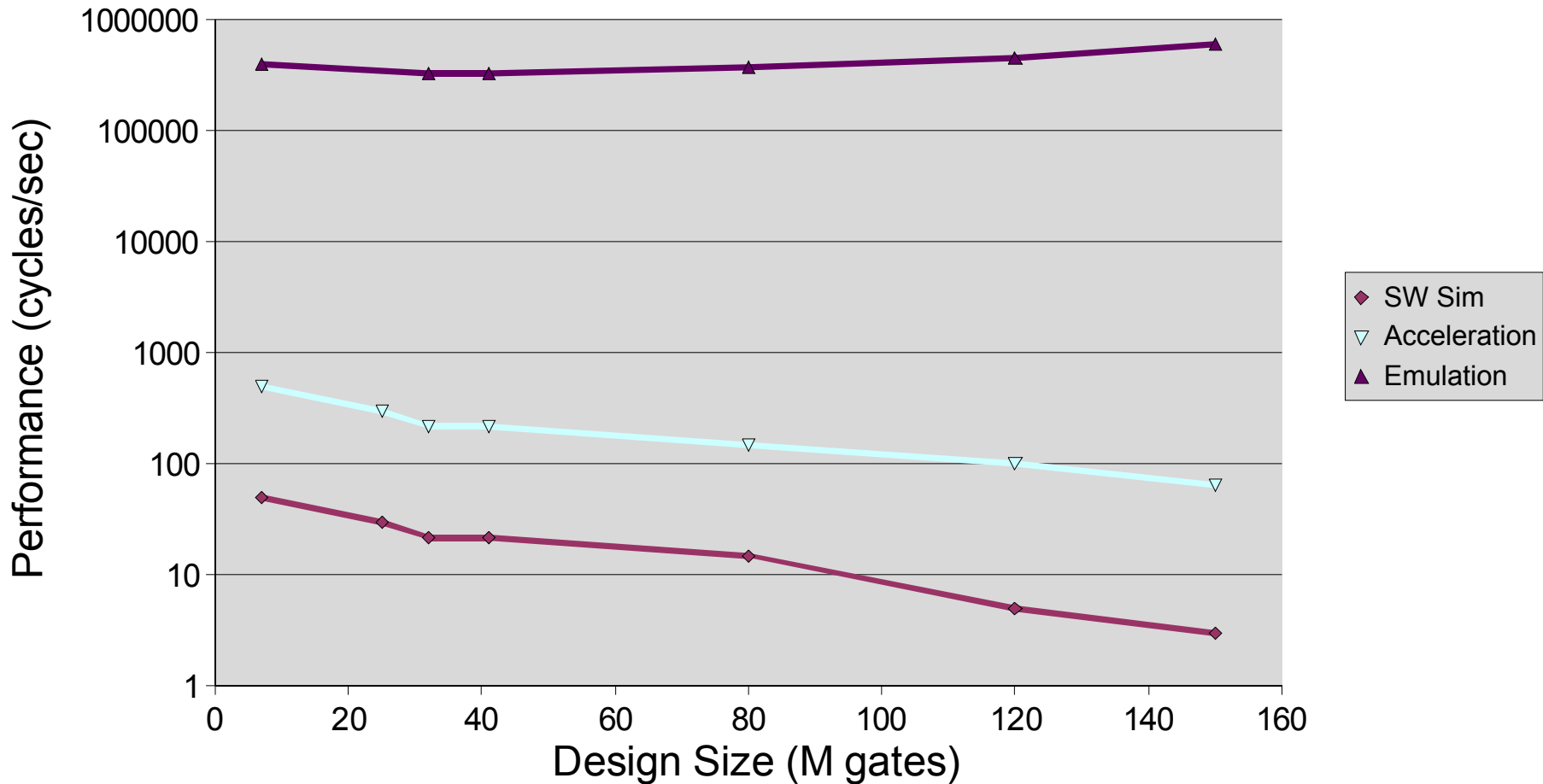
# When you put everything together and your simulator comes to a crawl....

Who do you call?



## Emulators

# Design Size Impact on Sim Speed



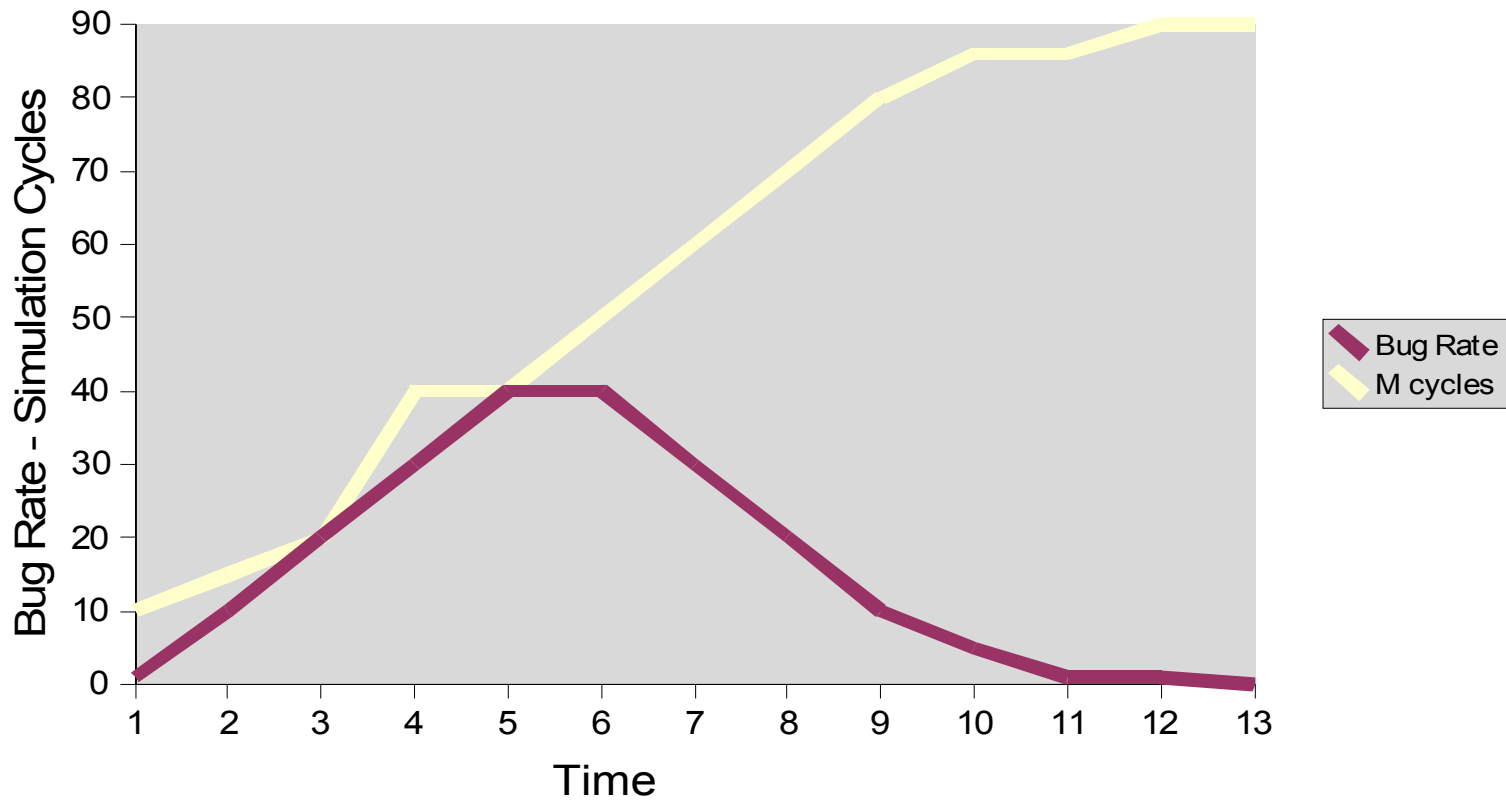
# When you need to run millions of cycles to catch those nasty deep corner case bugs....

Who do you call?



Emulators

# Simplified Bug Find Rate



# When you need to boot firmware, and Solaris....

Who do you call?



**Emulators**

Simulation - ~27years  
Emulation - 8.5hours

# When you need to run real world PCIE, ENET IO traffic on your SoCs....

Who do you call?



Emulators

# Emulation Resources – at a glance

Walk



SW Simulator

26.7 Years

Run



Competitor X

2.6 Years

Drive



Xtreme Server

2Days19Hrs

Fly



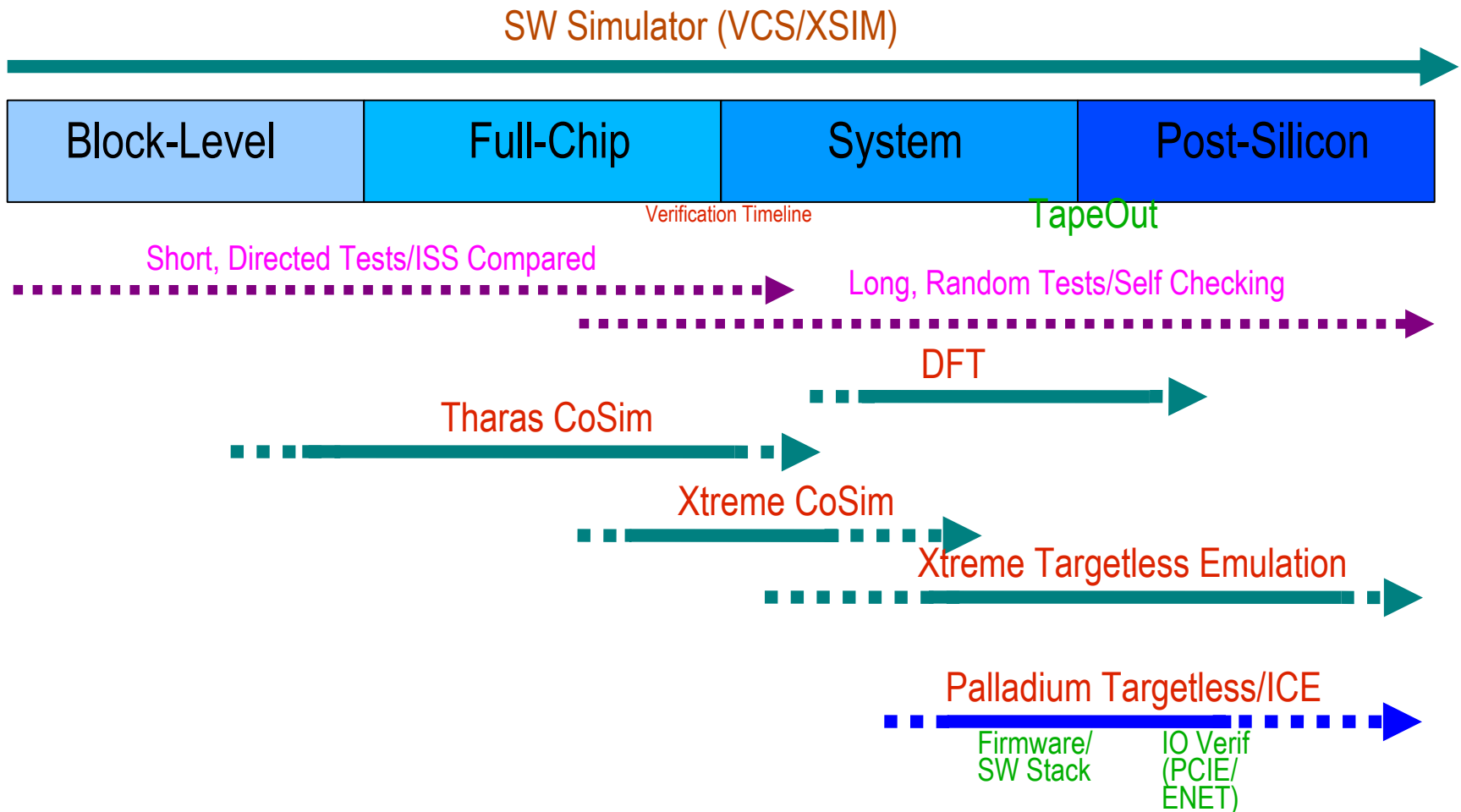
Palladium2

8 Hrs 30mins

Solaris  
Boot  
Time

Flexibility: Supported RTL, TestBench constructs

# Usage Model



# Emulation Verification:

*Get System HW/SW right the first time:*

- Prevent Functional Bug escapes (reduce Silicon re-spins - find bugs before tape-out)
- Facilitate early SW Development and System Integration
- Aid Post-Silicon Debug & Fix Validation

# Planning for Success

- Setup Emulation Environment early -
  - Create technology-awareness within team early in design phase
  - Decide Usage mode – co-sim, targetless, in-circuit emulation
  - Minimize learning curve - integrate into existing simulation flow
  - Not everything can be run on the emulator – prioritize & plan usage
- Reduce Time-to-Model Build -
  - Apply RTL enforcement (use lint, emulator tools);
- Minimize Modeling Issues
  - Array Modeling Methodology – abstract higher, make it “synthesizable”, race free
  - Optimize for Capacity and Performance: Eliminate non-functional models, abstract low-level details, minimize and align clocks
- Simplify Debug
  - Implement critical-set of Monitors for acceleration
  - Invest in debug tools to ease the debug complexity
  - Do not use it as yet another simulator (minimize waveform dumps)

Maximize ROI.

# HW Emulation Results

- Initial design bringup in co-simulation mode with ISS
- Target-less emulation for fastest throughput - trillions of cycles
- Ran really long directed tests
- Ran a number of self-checking random code generators to target tests to specific functionality – some tests run for days
- Reset Sequence testing, RAS Testing, On-Chip Debug test
- PCIE & ENET Testing using Speed Bridges
- JTAG Scan Testing using In-Circuit Emulation
- Motherboard bringup and test using In-Circuit Emulation
- Facilitated readiness of silicon test/debug tools
- Post-Silicon RTL bug fix validation

# Summary

- Exponential complexity with large SoCs
  - > multi-core,
  - > multi-threads,
  - > complex IOs
- HW Emulation is a must
  - > Traditional SW simulators alone are not enough
- Cost is justified in big scheme of product development