

Design Verification Research and Teaching

Kerstin Eder

Design Automation and Verification

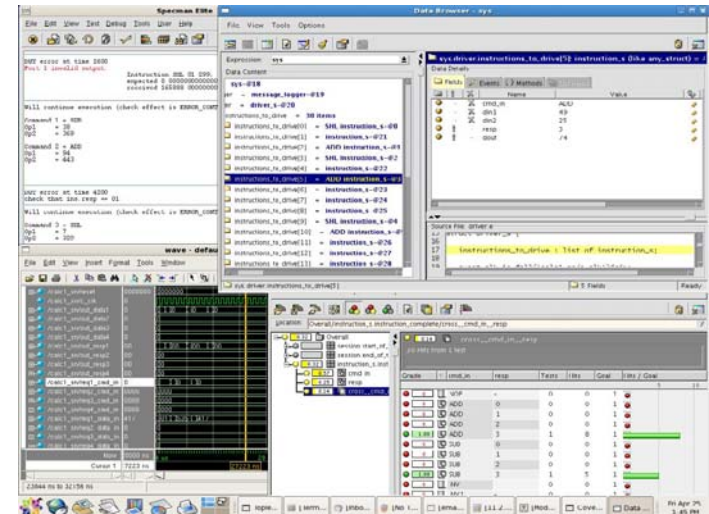
COMSM0115: Design Verification

Aim:

“To familiarize students with the routine tasks and the latest techniques in design verification, and to give them the theoretical background plus some of the practical skills expected from a professional design verification engineer.”

Syllabus

- **Introduction** to HW Design Flow and Functional Verification
- **Verification Flow and Tools**
- **Traditional simulation-based Verification:**
 - basic testbench architecture, directed testing, driving & checking tutorial
- **Verification Planning Process**
- **Coverage:**
 - metrics: structural, functional, analysis, need to combine metrics
- **Automation for Verification:**
 - constrained pseudo-random stimulus generation
 - self-checking testbenches
- **Coverage Driven Verification**
- **Assertion Based Verification**
- **Functional Formal Verification**



Design Verification Research

Exploiting state-of-the-art techniques from other areas of CS to advance Design Verification

- Formal specification, refinement, derivation and verification by mathematical proof
- Reassessing processor design decisions – impact on verification
- **Coverage Directed Test Generation:**
 - Formal approaches
 - Feedback-based approaches – machine learning
 - Methodology development for coverage balancing
- **Industrial Collaboration** with:
 - IBM Research Labs in Haifa (Israel)
 - Local semiconductor industry: STM, Infineon, Clearspeed, Xmos, BRCM, Icera etc
 - EDA: Cadence and Mentor Graphics

Opportunities to get involved

- **Undergraduate student projects**
 - Final year project BSc:
 - 400h (40 CP), part-time, October to May
 - Final year project MEng:
 - 400h (40 CP), full-time, February to May
- **MSc student projects**
 - 200h (20 CP), part-time, February to May
 - 600h (60 CP), full-time, June to September
- **PhD**
 - 3 years 6 months full-time research
- **EngD**
 - 4 years full-time research and professional training
 - 75% of time spent in industry
 - Portfolio-based



Get involved:

Contact Kerstin.Eder@bristol.ac.uk to explore collaboration opportunities

Ramaram Naresh (MSc AMSE student at University of Bristol)

Email ID : nr8627@bristol.ac.uk

- **Experience** : Worked as Member Technical staff in GD Micro Systems Pvt Ltd for THREE plus years.
- **Interested in** : SOC Verification, Analog & Mixed signal design.
- **Domain Expertise** : SOC Verification, Reference Verification Methodology & AMBA AHB/APB bus systems.
- **Projects Done** : **Dual core 2 million gate count System-on-chip using 90nm** technology, AHB Verification IP using VERA.
- **Role** : Verification of chip at block, system and production level.
- **Languages** : C, C++, Verilog, Unix, Perl.