

Progressive migration from 'e' to SystemVerilog : Case Study

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Agenda

- Briefly describe application space
- Describe advantages/challenges/solutions in staging the migration
- Describe an approach for allowing multiple vendor simulation solution
- Conclusions

TIUK SERDES

Design Team

- TIUK is part of TI ASIC business unit
- Design SERDES
 - very high speed low swing IOs
 - 12.5GBPs on 65nm technology
- Complex mixed signal designs
 - > 1 million CMOS elements
 - Very high speed digital
 - Bespoke DSP algorithms to recover data from highly lossy transmission lines
 - Complex high speed analog
 - PLLs, RX/TX analog front ends
 - 6GSS very low power ADCs
- E based verification environment
 - Developed/used for > 8 years
 - Many successful tape outs

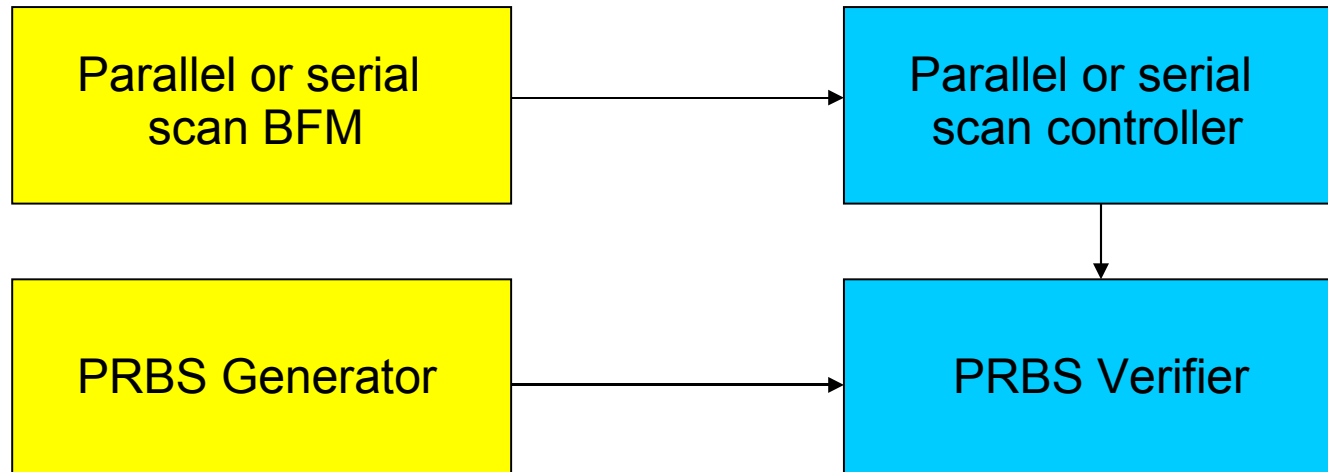
Staged Migration

- Positives
 - Reduced risk
 - Allows learning in a small constrained environment
 - Team members can be trained in small groups to avoid all team out of office at same time
 - We don't have the resource to stop everything to write a new testbench in one go
 - Resource requirements amortized over several projects
- Negatives
 - Takes longer to gain benefits
 - Specman/e must coexist with SVTB!

Proof of Concept

Specman Testbench

Verilog DUT



PRBS = Psuedo Random Binary Sequence

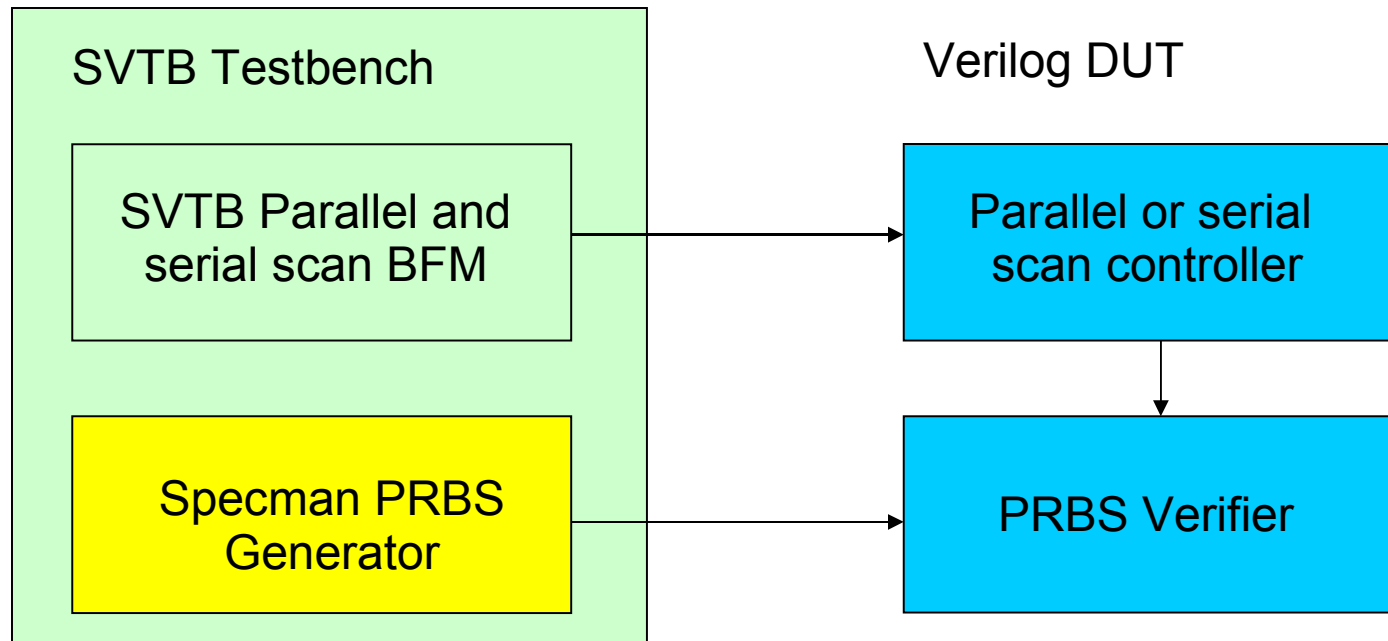
Technical Challenges with Migration

- Specman/e and SVTB may both need to progress time
 - Who is the master?
 - How does the time wheel work?
- Some parts of the testbench in E others in SVTB
 - 2 testcases!
 - How do you communicate between the 2 different parts?

Solutions

- SVTB is the master
- Testcase written in SVTB as if everything has been converted
- SVTB tells remaining E code what to do
- Partition testbench to minimize communications between SVTB and E
- Pass information via verilog
 - SVTB sends information to verilog via an interface
 - Extend E units to add code to extract information from verilog instead of from other E units/structs

Proof of Concept After Conversion



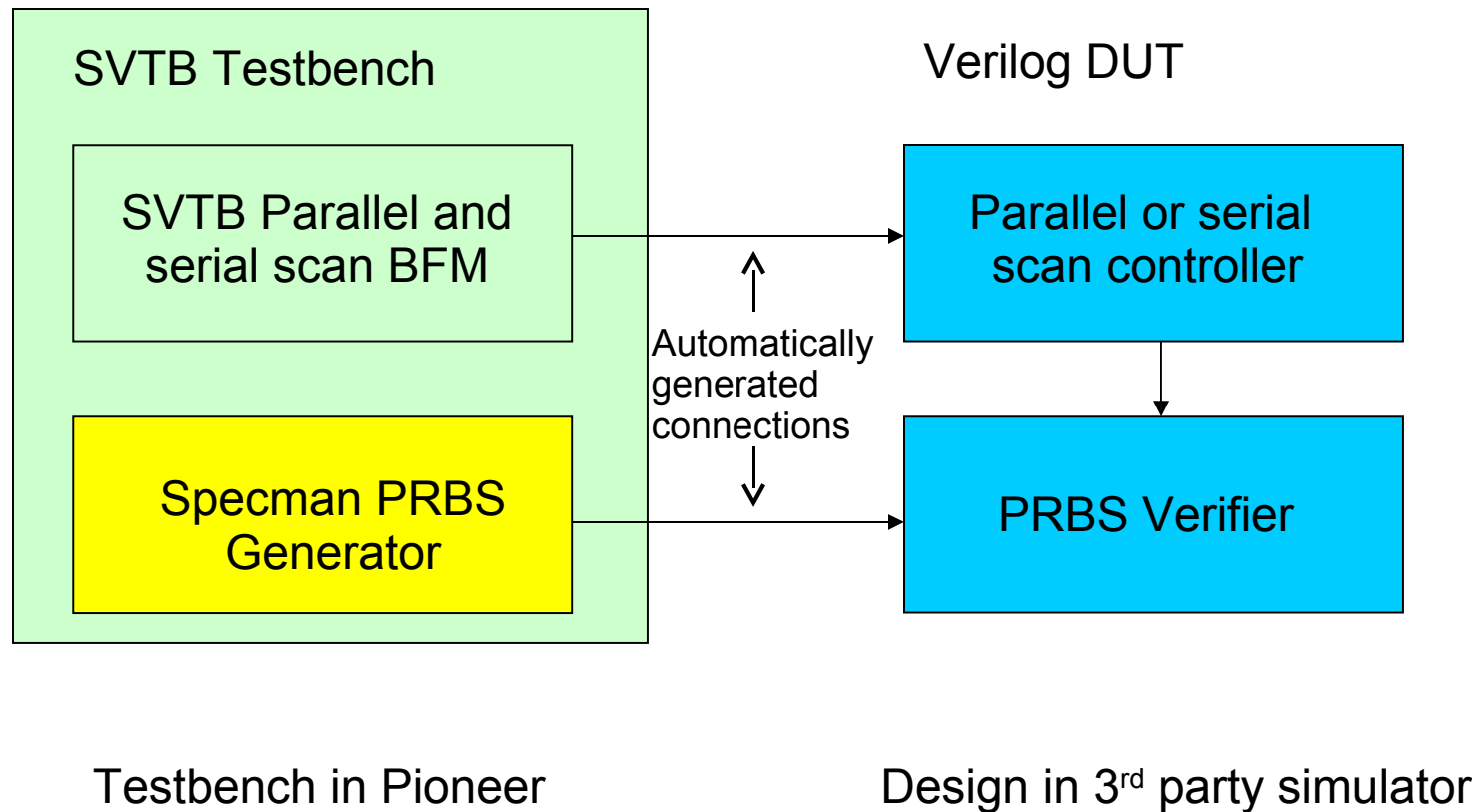
Multi-simulator support

- TIUK provides hard IP to internal/external customers
- Provide verilog models for customers to simulate at chip level
- Customers can use all 3 major verilog simulators and verilog model must be verified on these simulators
- E allowed testbench to be used with all 3 simulators without modification
- SVTB is currently 1 standard language with at least 3 dialects
 - Use lowest common denominators? Yuk!
- Variable legal latency through IP means must use intelligent testbench and not vector playback

Pioneer Testbench tool (SNPS)

- Allows testbench to exist in Pioneer only
- Allows design to exist in other simulator
- Automatically (seamlessly) connects between testbench and DUT
- Uses PLI so a performance overhead exists
 - Only use for model QC on other simulators, not as part of design development/verification work
- As SVTB implementation stabilizes across vendors need for Pioneer will reduce

Pioneer



Conclusions

- Have presented staged migration from E to an SVTB
 - Staged migration minimizes risk and amortizes conversion costs across multiple projects
- Pioneer enables multi-vendor IP simulation
 - avoids need to use lowest common denominator of the vendor implementations

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Questions?