



# Constrained-Random Thoughts on Design and Verification of Advanced DSP Blocks for Next-Generation Handsets

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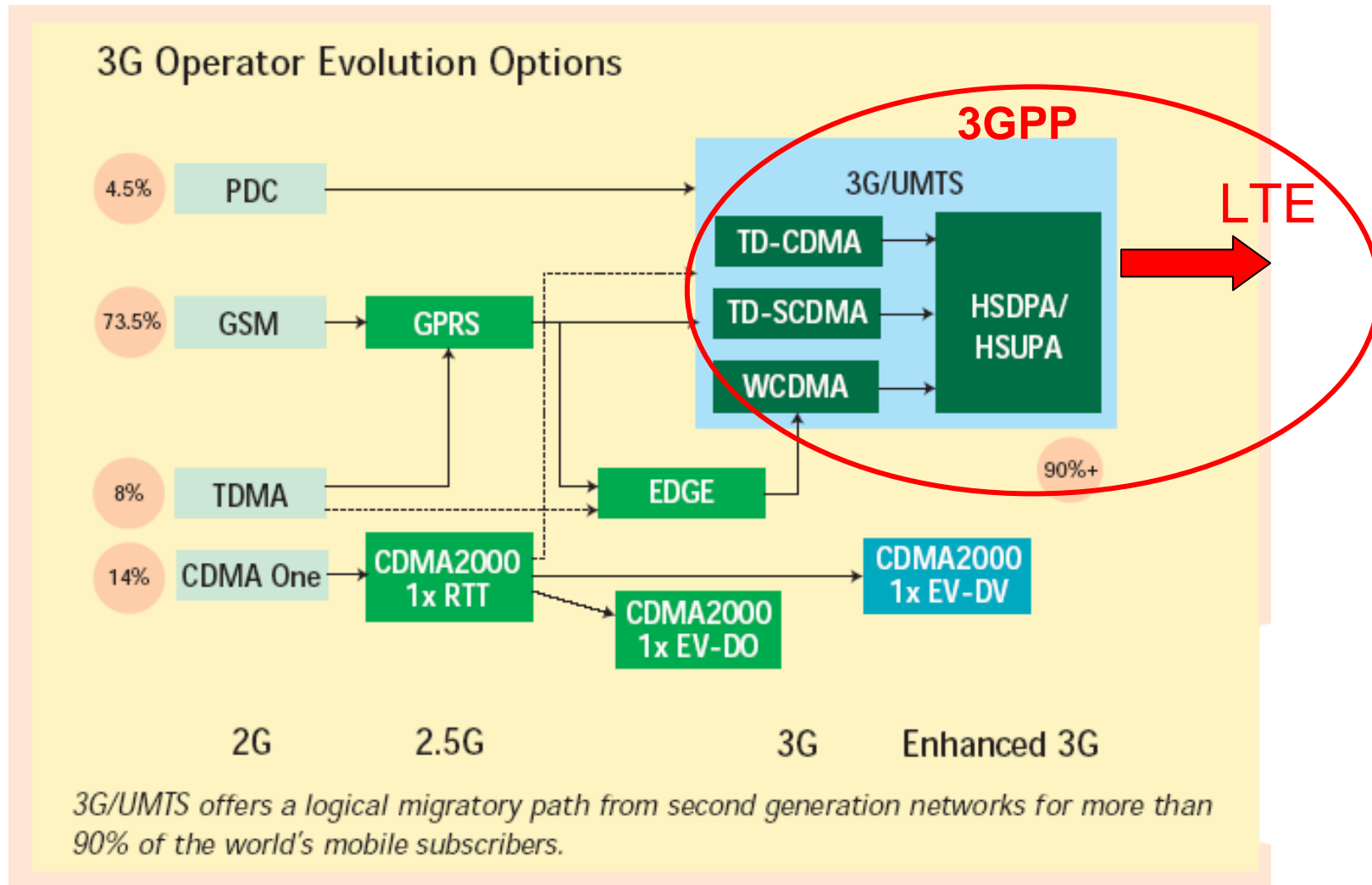
# Overview

- Our Team
  - Who are we and what are we working on?
- Our Design and Verification Flow
  - The “obvious but traditional” way
  - The “new and improved” way
- Conclusions

# Who Are We?

- MediaTek Wireless, RF & Wireless Systems (RFWS): Cellular handset business of Analog Devices, which was acquired by MediaTek in January '08.
  - Provider of chipset solution for 2G/3G handsets, including GSM/GPRS, EDGE, WCDMA, TD-SCDMA
- MediaTek is a fabless semiconductor provider with headquarters in Taiwan

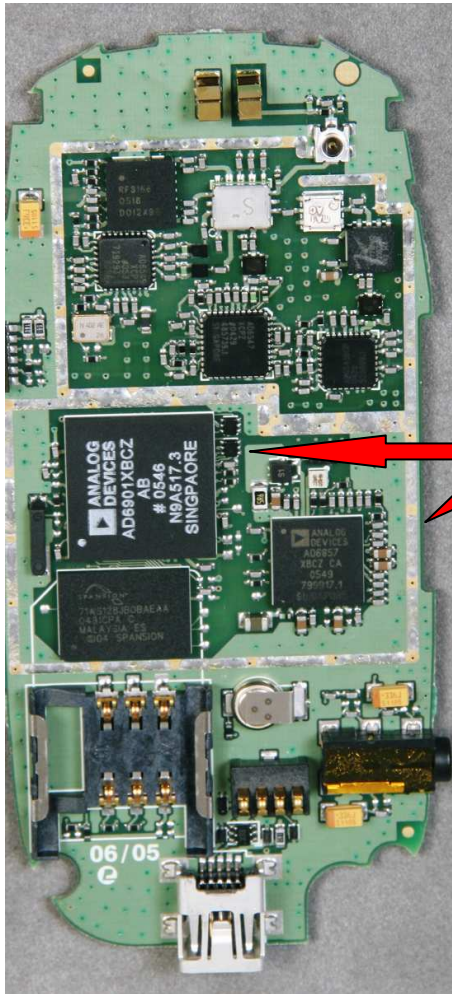
# What are we working on?



# Next-Generation Handsets

- Powerful application processors and memory technologies enable advanced applications ....
  - “The Internet on your phone”: Productivity apps, Multimedia, Location services, Games, VOIP, ...
- But this requires lots of bandwidth ...
- And to provide this bandwidth wirelessly, physical layer processing for 3G and beyond is exponentially more complex than 2/2.5G technologies
  - Conventional programmable DSPs have run out of steam
  - Requires hardware acceleration for key modem blocks: RAKE, equalizer, filters, MIMO, H-ARQ, turbo/Viterbi decoders, ...

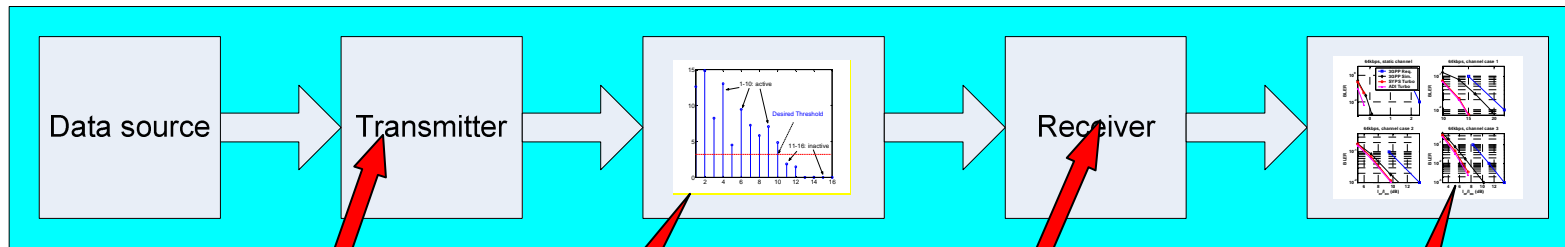
# Modem Technology for Next-Generation Handsets



- Othello Radio Technology
  - GSM/EDGE
  - WCDMA, **TD-SCDMA**
- Analog/Mixed-Signal Baseband (ABB) Technology
  - Integrated Audio/Power Management
- SoftFone Baseband Architecture
  - Multi-core (MCU/DSP)
  - Modem accelerators for GSM/GPRS, EDGE, WCDMA, **TD-SCDMA**
- System-in-Package (SIP) and System-on-Chip (SoC) integration
- Software, Tools, Support



# Algorithms: Verifying/Validating Link-Level Models



## Transmission Parameters

- Error-Correction Coding
- Rate-matching
- Modulation
- Spreading

## Environment Parameters

- Channel conditions (multi-path fading profile, SINR)

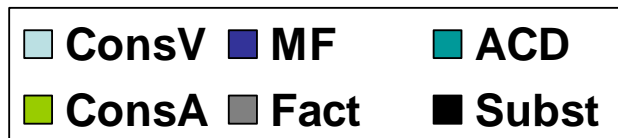
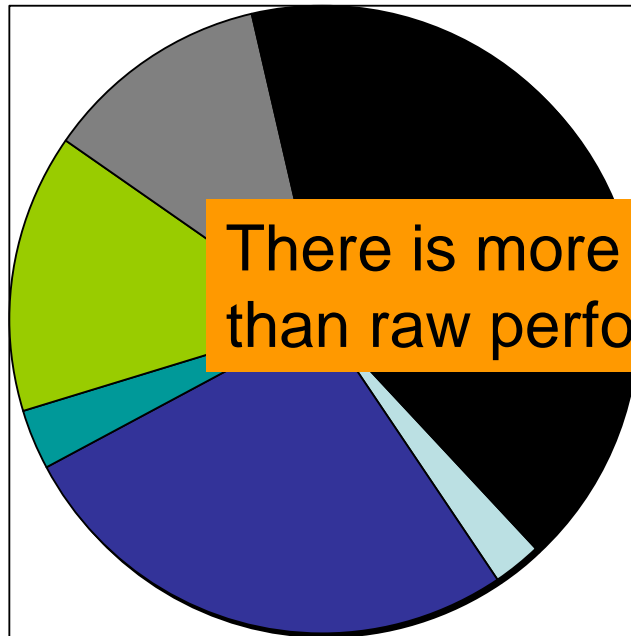
## Receiver algorithms

- Channel estimation
- Demodulation
- Detection
- Quantization effects

## Key Performance Indicators

- Block Error Rate (BLER)
- Effective throughput

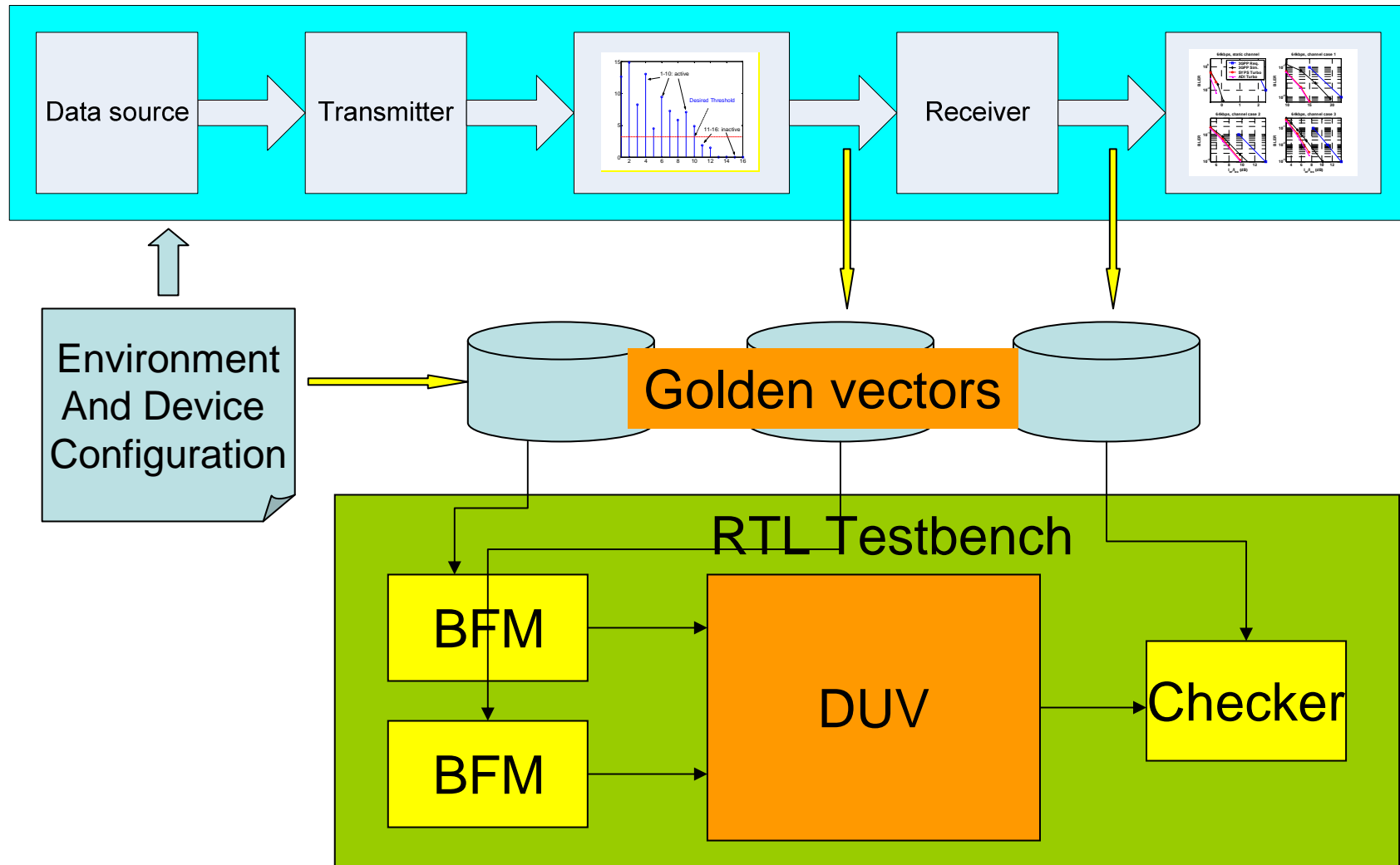
# Architecture: HW/SW Partitioning



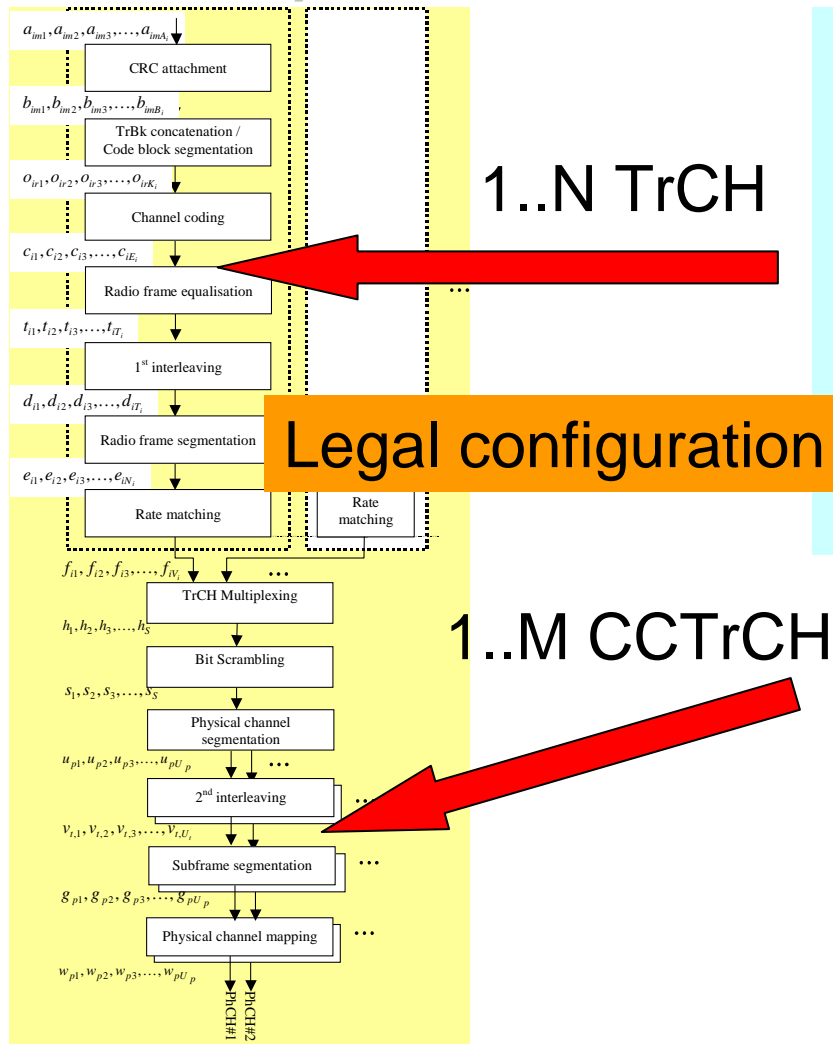
There is more to HW/SW partitioning than raw performance

- Start from DSP executable
  - MIPS, memory, power
- Assign to HW
  - Cycle budget busters
  - Short/long word lengths
- Assign to SW
  - Light workloads
  - New standards
  - Standard word length (16, 32 bits)
  - 3<sup>rd</sup> party IP

# Verification: The Obvious but Traditional Way



# Device Configuration Parameters (TrCH, CCTrCH)



Legal configuration space is huge interval (TTI)

- CRC size
- Transport block size, number of transport blocks
- Channel coding: Turbo, convolutional (rate-1/2, 1/3)
- Rate matching parameter

- Physical Channel parameters
  - Timeslot
  - Slot format
  - UE codes

Source: 3GPP TS25.222

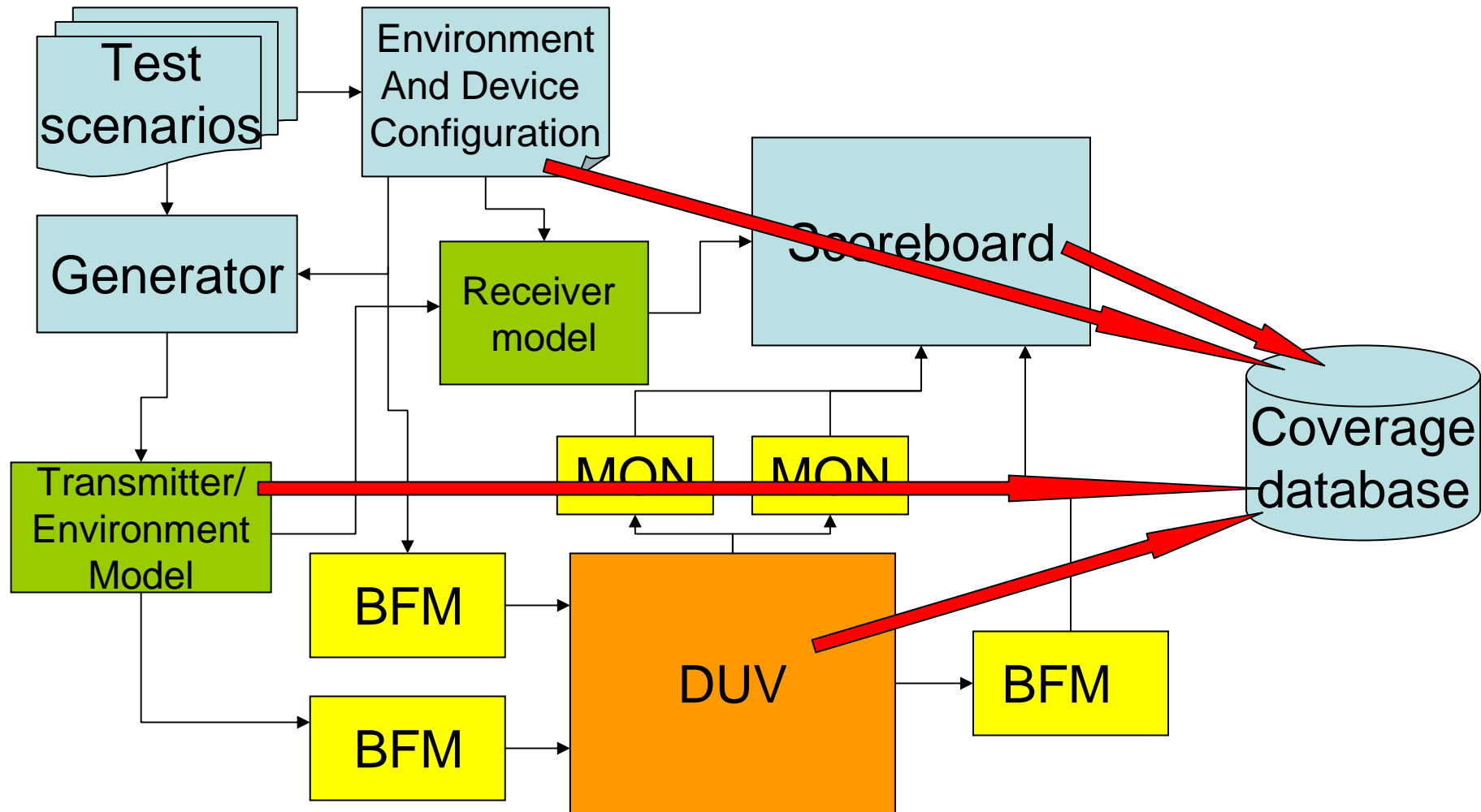
# Problems with the Obvious Way

- Full coverage requires massive amounts of vectors
- Verification environment is static, can't react to DUV
- High-level environment and device configuration parameters are lost
- Link-level environment is usually not set up for complex and non-typical scenarios
- Not all device behaviors fully modeled in link-level environment
- Your system team will end up hating you!

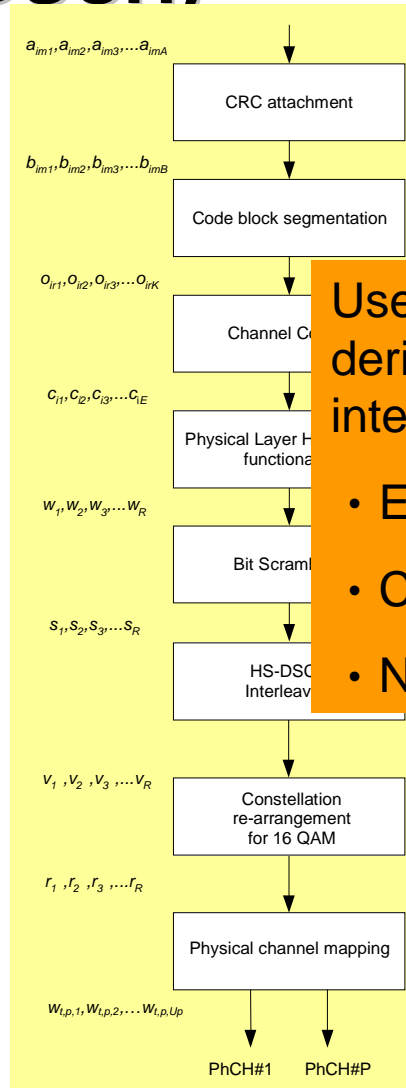
# Verification: The New and Improved Way

- SystemVerilog
  - Big step up from verilog
- Stimulus
  - Directed vectors (compliance, bring-up)
  - Constrained-random scenarios (coverage-driven)
  - Embedded transmitter models (DPI)
- Checking
  - Data checking with embedded reference models (DPI)
  - Protocol checking with monitors/assertions
- Coverage
  - Code coverage
  - Functional coverage
    - Cover properties (embedded in RTL)
    - Covergroups (embedded in testbench, automatically generated from XML register database)

# Constrained-Random Verification Environment



# HSDPA Device Configuration Parameters (HS-DSCH)



```
// Ki = code block size
// Ci = number of code blocks
// Fi = number of filler bits
// Z = max. code block size
// Yi = encoded data size
constraint xxx_constraint {
    7 5111
```

Use constraints to compute derived parameters, define interesting testcases

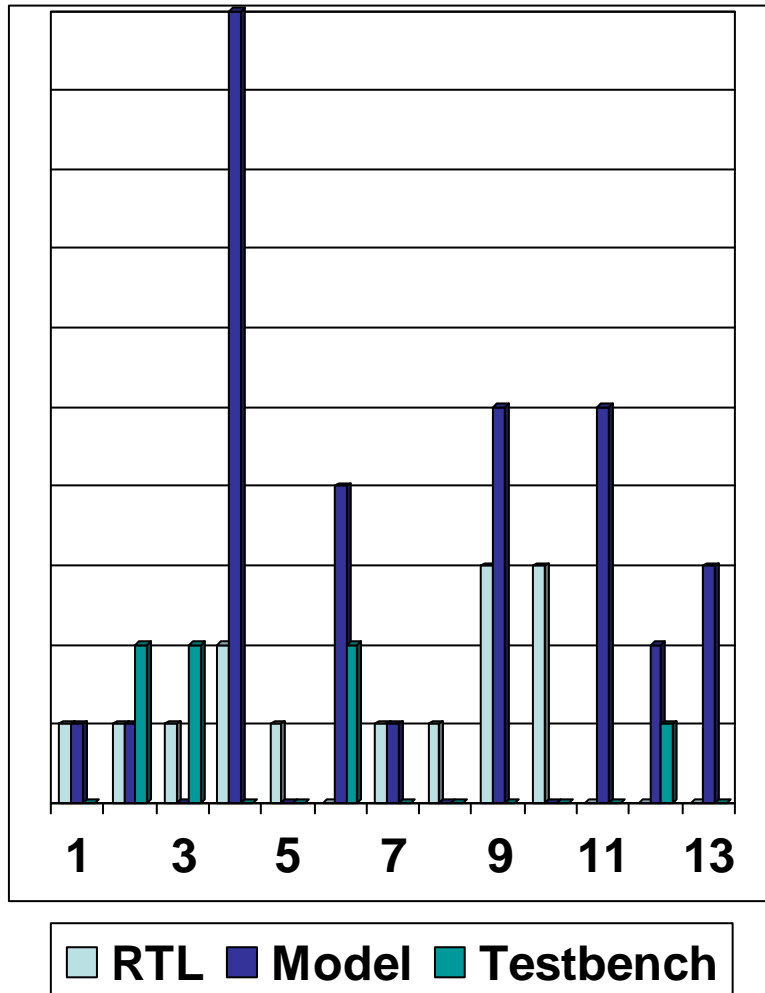
- Encoder/decoder filler bits
- Code block size
- Number of code blocks

```
// Equations for Ki
Ki <= Z;
Ki * Ci >= Xi;
Ki * Ci < Xi + Ci;
//(Xi < 40) -> Ki == 40;
}
```

- Transport block size
- Rate-matching parameters
- Modulation type
- Constellation version
- Spreading factor
- Active physical channels
- Active timeslots

Source: 3GPP TS25.222

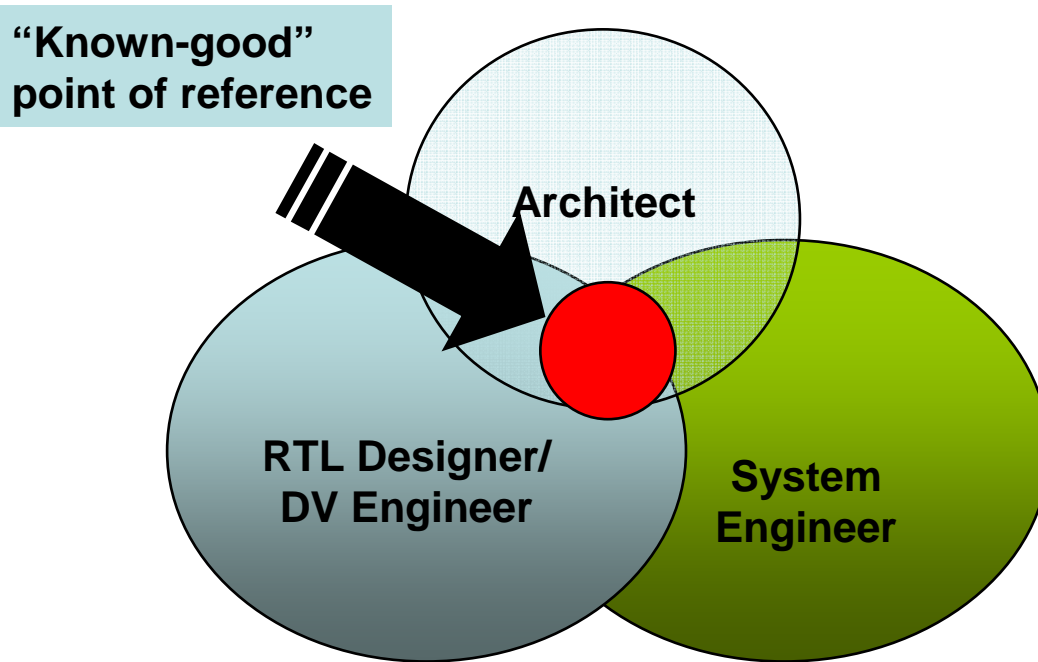
# Result: Bug Tracking for a “reused” IP



- RTL was reused in different configuration
- Model was adapted to TDD standard
- Testbench was “borrowed” from previous project

- Week 1: Designer testbench
- Week 2-3: Directed
- Week 4-8: Random+directed
- Week 9-13: Constrained-random

# Executable reference models are key !



- No ambiguities: Architect, RTL/DV Engineer and System Engineer all use the same golden reference model
  - Eliminates guesswork of interpreting written specifications
  - Eliminates rework by reusing system model for RTL/DV and system integration

# Conclusions

- Next-generation handsets have sophisticated DSP acceleration that gets progressively harder to verify
- Don't use your system team as a generator of infinite stream of testcases, but as a source of high quality reference models
- Build constrained-random verification environment incorporating reference models for testcase generation and data checking
- We've successfully taped out 2 chips with this methodology (the first is in production, the second under customer eval)

# MEDIA TEK

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